01-27-00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Pierre C. Fazan et al.

Title: METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS

Attorney Docket No.: 303.434US2

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X **DIVISIONAL** of prior Patent Application No. 08/572,392 (under 37 CFR § 1.53(b)) comprising:
- X Specification (25 pgs, including claims numbered 1 through 27 and a 1 page Abstract).
- X Formal Drawing(s) (33 sheets: Figs 1-11 original and Figs. 12-28 from co-filed Preliminary Amendment).
- X Copy of signed Combined Declaration and Power of Attorney (3 pgs) from prior application.
- X Copy of Revocation and Power of Attorney (2 pgs.) from prior application.
- X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
- X Check in the amount of $1,854.00 to pay the filing fee.

X Prior application is assigned of record to Micron Technology, Inc..

X Information Disclosure Statement (1 pgs), Form 1449 (2 pgs). References NOT enclosed, cited in prior application.

X Copy of Preliminary Amendment (25 pgs) as filed in parent application (Figs 12-28 included with Formals.)

X Supplemental Preliminary Amendment (6 pages).

X Return postcard.

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	50 - 20 =	30	x 18 =	$540.00
INDEPENDENT CLAIMS	11 - 3 =	8	x 78 =	$624.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
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TOTAL				$1,854.00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Pierre C. Fazan
Viju K. Mathews

Parent Serial No: 08/390,336

Parent Filed: 02/17/95

For: A METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS

Docket Number: 92-0501.02

Paper No: 1

December 14, 1995

Commissioner of Patents
& Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

In the specification:

Kindly delete the abstract page and insert the following page:

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A METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS

The invention is a storage cell capacitor having a storage node electrode comprising a barrier layer interposed between a conductive plug and an oxidation resistant layer. A thick insulative layer protects the sidewall of the barrier layer during the deposition and anneal of a dielectric layer having a high dielectric constant.

The method comprises forming the conductive plug in a thick layer of insulative material such as oxide or oxide/nitride. The conductive plug is recessed from a planarized top surface of the thick insulative layer. The barrier layer is formed in the recess and the top surface of the barrier layer is recessed below the top surface of the oxide or oxide/nitride layer. The process continued with a formation of an oxidation resistant conductive layer and the deposition of a further oxide layer to fill remaining portions of the recess. The oxidation resistant conductive layer is planarized to expose the oxide or oxide/nitride layer and the oxide layers are then etched to expose the top surface and vertical portions of the oxidation resistant conductive layer.

Next a dielectric layer having a high dielectric constant is formed to overlie the storage node electrode and a cell plate electrode is fabricated to overlie the dielectric layer.--.

On page 2 before the first line please insert:

--This is a continuation-in-part of co-pending application serial no. 08/390,336 filed on 2\17\1995 which is a continuation of serial no. 08/044,331 filed on 4/2/1993, now abandoned.

A continuation having docket no. 93-0320.02 of serial no. 08/313,677 filed on 9/27/1994 which is a divisional of serial no. 08/104,525 filed on 8/10/1993 and which may contain similar material is co-pending and is filed simultaneous herewith.--.

On page 6, line 4 after "issues." please insert the following paragraphs:

--The invention includes a storage node capacitor having a storage node electrode comprising a barrier layer interposed between a conductive plug and an oxidation resistant conductive layer and the method for fabricating the same. A thick insulative layer protects the sidewall of the barrier layer during the deposition and anneal of a dielectric layer having a high dielectric constant.

In one preferred implementation the method comprises forming the conductive plug in a thick layer of insulative material such as oxide or oxide/nitride. The conductive plug is recessed from a planarized top surface of the thick insulative layer. The barrier layer and the oxidation resistant layer are formed in the recess. A portion of the thick insulative material is removed to expose portions of the oxidation resistant layer. Remaining portions of the thick insulative material continue to encompass the barrier layer.

Next a dielectric layer having a relatively high dielectric constant is formed to overlie the storage node electrode and a cell plate electrode is then fabricated to overlie the dielectric layer. In this preferred implementation, since the barrier layer is protected during the formation of the dielectric layer by both the oxidation resistant conductive layer and the thick insulative layer there is little or no oxidation of the barrier layer or the contact plug, thereby maximizing capacitance of the storage node and reducing high contact resistance issues.

In one particular preferred embodiment, the barrier layer is tantalum or another material which experiences no oxidation during the formation of the storage cell capacitor. The oxidation resistant conductive layer is preferably a non-oxidizing conductive material such as platinum. The dielectric layer is preferably $Ba_xSr_{(1-x)}TiO_3$ [BST].

The insulative layer and the oxidation resistant layer protect the barrier layer from oxidizing during the deposition and anneal of the BST thereby also eliminating oxidization of the conductive plug. By minimizing or eliminating oxidization of the barrier layer and the conductive plug capacitance is maximized.--.

On page 7, line 15 after "capacitor." please insert the following paragraphs:

--Figure 12 is the cross sectional view of Figure 5 following the formation of a recess in the oxide layer.

Figure 13 is the cross sectional view of Figure 12 following the deposition of a barrier layer.

Figure 14 is the cross sectional view of Figure 13 following an etch back of the barrier layer.

Figure 15 is the cross sectional view of Figure 14 following a deposition of an oxidation resistant layer.

Figure 16 is the cross sectional view of Figure 15 following a further oxide deposit and the planarization of the oxide and the oxidation resistant layer.

Figure 17 is the cross sectional view of Figure 16 following an etch back of the oxide deposits.

Figure 18 is the cross sectional view of Figure 17 following formation of a dielectric layer and cell plate layer.

Figure 19 is the cross sectional view of the capacitor made by the process described in steps 2-5 and 12-19.

Figure 20 is the cross sectional view of Figure 12 following the formation of a conductive layer.

Figure 21 is the cross sectional view of Figure 20 following removal of non silicide portions of the refractory metal (or metal nitride) layer.

Figure 22 is the cross sectional view of Figure 21 following the formation of a barrier layer.

Figure 23 is the cross sectional view of Figure 22 following an etch back of the barrier layer.

Figure 24 is the cross sectional view of Figure 23 following a deposition of an oxidation resistant layer.

Figure 25 is the cross sectional view of Figure 24 following a further oxide deposit and the planaraiztion of the oxide and the oxidation resistant layer.

Figure 26 is the cross sectional view of Figure 25 following an etch back of the oxide deposits.

Figure 27 is the cross sectional view of Figure 26 following formation of a dielectric layer and cell plate layer.

Figure 28 is the cross sectional view of the capacitor made by the process described in steps 2-5, 12, and 20-28.--.

On page 14, line 3 after "claimed." please insert the following paragraphs:

--In the crown embodiment of the invention the initial formation of the capacitor is accomplished according to the steps depicted in Figures 2-5 and described in reference to Figures 2-5. The process continues with steps 12-19. Layers corresponding to similar layers of the previous embodiments shall be numbered the same.

Referring now to Figure 12, an upper portion of each polysilicon plug 65 is removed during a dry etch in order to form recesses 70. Typically, this etch back is 50 to 400 nano meters (nm). In a case where the polysilicon plugs 65 are formed during a selective silicon growth it is possible to form the recess 70 by controlling the growth.

Referring to Figure 13, a tantalum layer 75 is formed by a chemical vapor deposition (CVD) or a sputtering process, which may be performed at room temperature. The tantalum layer 75 provides a barrier against silicon diffusion of the polysilicon plug during subsequent high temperature anneals. Other materials capable of prohibiting silicon diffusion may be used in place of tantalum such as, for example: titanium nitride, TaN, Ti, RuO_2, and Ru.

Referring to Figure 14, the tantalum layer 75 shown in Figure 7 is etched back in order to expose the oxide layer 40 and in order to retain tantalum 75 in recesses 70 overlying the polysilicon plugs 65. The tantalum layer 75 should be recessed below a top surface of the exposed oxide layer 40. The etch back may be preceded by a planarization to

remove the tantalum overlying the oxide layer 40. Portions of the oxide layer 40 may be planarized during this step. The thickness of the initial tantalum layer 75 is preferably such that after the etch back/planarization or the etch back the portion of the tantalum layer 75 retained in the recess 70 has a depth sufficient to inhibit silicon diffusion of the polysilicon plugs 65. It can be seen that at this juncture of the process only the upper surface of the tantalum layer 75 is exposed and the tantalum sidewall 80 is protected by the oxide layer 40.

Referring now to Figure 15, a platinum layer 85 is formed by CVD or a sputtering technique. The platinum layer 85 overlies the tantalum layer 75. Since the platinum layer 85 is resistant to oxidation it provides an excellent surface for the deposition of the high dielectric constant material. Other materials which are resistant to oxidation may be used in place of the platinum. For example, RuO_2 and TiN, as well as other non-oxidizing materials may be used. In this embodiment of the invention the platinum layer 85 is relatively thin, approximately 50nm thick, although other thicknesses may be used without departing from the spirit and scope of the invention. The thickness of the platinum should be great enough to substantially protect the tantalum layer 75 against oxidation during BST deposition.

In Figure 16 oxide 86 is deposited into the recess 70, and the structure is planarized to remove portions of the platinum layer 85 overlying the oxide layer 40.

In Figure 17 the oxide layers 40 and 86 have been etched to expose a vertical sidewall of the platinum layer 85 and the upper surface of the platinum layer 85. It is necessary to retain a sufficient quantity of oxide 40 at the lower sidewall of platinum layer 85 to eliminate the possibility of oxidizing the tantalum layer 75. In order to retain sufficient oxide 40 while at the same time exposing the upper surface of the platinum layer 85 the densification of the oxide 86 must be less than the densification of oxide 40 in order for the oxide layer 86 to etch at a faster rate than the oxide layer 40.

Now the fabrication of the crown embodiment the storage node electrode is complete. Although the polysilicon plug 65 is often thought of as an electrical interconnect interposed between the substrate and the storage node electrode, it can be thought of as a portion of the storage node electrode itself.

Figure 18 depicts initial formation of the storage cell capacitor following a deposition and anneal of a dielectric layer 90 overlying the platinum layer 85. The dielectric layer 90 is typified as having a high dielectric constant. The storage cell capacitor fabrication is completed with the sputter or CVD of a 50 to 200nm thick cell plate layer 95

to form a cell plate electrode. The cell plate layer 95 is typically platinum, TiN or some other conductive material.

Following the deposition of the dielectric layer 90 and the cell plate layer 95 the storage cell capacitor is patterned and the cell plate layer 95 and the dielectric layer 90 are etched to complete the fabrication of the storage cell capacitor as shown in Figure 19.

Among the suitable materials for a dielectric layer having a high dielectric constant are $Ba_xSr_{(1-x)}TiO_3$ [BST], $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$ [PZT], $(Pb,La)(Zr,Ti)O_3$ [PLZT], $(Pb,La)TiO_3$ [PLT], KNO_3, and $LiNbO_3$. In currently envisioned embodiments BST is the preferred material and is deposited at a thickness range of 30nm-300nm by RF-magnetron sputtering or CVD. The tantalum layer 75 is not oxidized during the application of a high temperature anneal due to the fact that it is protected on its sidewall by the oxide layer 40 and that it is protected on its upper surface by the platinum layer 85.

The process can be continued or modified to accommodate the steps described in U.S. patent 5,168,073, previously incorporated by reference, for providing electrical interconnection between a plurality of capacitors thus formed.

By utilizing the method of the invention, a high density memory device is provided featuring a stacked capacitor formed in a compact area as a result of a dielectric layer having a high dielectric constant. The stacked capacitor of the invention retains storage node integrity during an anneal of the dielectric layer.

In an alternate embodiment of the crown embodiment, the deposition of the tantalum layer is preceded by a deposition of a titanium barrier layer 100, see Figure 20. A thermal anneal is performed. The titanium in contact with the polysilicon plug reacts with the polysilicon to form titanium silicide during the anneal. It is possible to perform the anneal in nitrogen. In this case the titanium still reacts with the polysilicon to form titanium silicide, and the titanium which is not in contact with the polysilicon plug reacts with the nitrogen to form TiN. In addition a thin layer of nitrogen is formed overlying the titanium silicide.

In addition to titanium, other metals including refractory metals may be used. These refractory metals may include W, Co, Ta, and Mo.

Alternately a metal nitride, such as TiN, may be deposited instead of a refractory metal. The refractory metal and the metal nitride are both capable of reacting with the polysilicon plug to form a silicide during an anneal.

Referring now to Figure 21, the non-silicide layer (the unreacted titanium, in the case of a non-nitrogen anneal, or TiN formed during the nitrogen anneal) and the thin layer of nitrogen formed overlying the titanium silicide 105 have been removed during a wet etch. The titanium silicide 105 overlying the polysilicon plug is retained during the etch.

The process is continued as shown in Figures 22-28 and the process corresponds to the process described with respect to Figures 13-19, respectively, of the previous embodiment with the exception that the barrier layer 75 is TiN in the present embodiment rather than tantalum which was used in the previous embodiment. However, tantalum, TaN, Ti, RuO_2, and Ru may be used.

The titanium silicide layer 105 lowers a contact resistance between the polysilicon plug 65 and the TiN layer 75.

The TiN layer 75 provides a barrier against silicon diffusion of the polysilicon plug and the titanium silicide layer during subsequent high temperature anneals.

Although a process has been described for forming the storage cell capacitor, it is apparent the process is equally applicable for the fabrication of other types of capacitors used in integrated circuits. It should also be apparent to one skilled in the art that changes and modifications, such as deposition depths, may be made thereto without departing from the spirit and scope of the invention as claimed.--.

In the Claims:

Kindly delete claims 1-27.

Please add the following claims:

--28. An electrode, comprising:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said insulative layer, wherein said first portion and said second portion are different materials.

29. The electrode as specified in Claim 28, wherein said second portion and said third portion are different materials.

30. The electrode as specified in Claim 29, wherein said first portion and said third portion are different materials.

31. An dynamic random access memory device, comprising:

an electrode which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said

insulative layer, wherein said first portion and said second portion are different materials.

32. The electrode as specified in Claim 31, wherein said second portion and said third portion are different materials.

33. The electrode as specified in Claim 32, wherein said first portion and said third portion are different materials.

34. An dynamic random access memory device, comprising:

a capacitor which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said insulative layer, wherein said first portion and said second portion are different materials.

35. The electrode as specified in Claim 34, wherein said second portion and said third portion are different materials.

36. The electrode as specified in Claim 35, wherein said first portion and said third portion are different materials.

37. The dynamic random access memory device as specified in Claim 34, further comprising a transistor.

38. The dynamic random access memory device as specified in Claim 34, further comprising:

a) a dielectric layer overlying said third portion; and

b) a cell plate electrode overlying said dielectric layer.

39. An electrode, comprising:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are different materials.

40. The electrode as specified in Claim 39, wherein said second portion and said third portion are different materials.

41. The electrode as specified in Claim 40, wherein said first portion and said third portion are different materials.

42. The electrode as specified in Claim 39, further comprising a fourth portion

interposed between said first and said second portions.

43. The electrode as specified in Claim 42, wherein the fourth portion reduces contact resistance between said first and said second portions.

44. The electrode as specified in Claim 39, wherein said first portion is a silicon contact.

45. The electrode as specified in Claim 39, wherein said second portion is a diffusion barrier layer prohibiting diffusion of atoms between said first and said second portions.

46. The electrode as specified in Claim 39, wherein said third portion is an oxidation resistant layer.

47. The electrode as specified in Claim 39, wherein said insulative layer surrounds a lower sidewall of said third portion.

48. A dynamic random access memory device, comprising:

an electrode which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are

different materials.

49. The electrode as specified in Claim 48, wherein said second portion and said third portion are different materials.

50. The electrode as specified in Claim 49, wherein said first portion and said third portion are different materials.

51. A dynamic random access memory device, comprising:

a capacitor which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are different materials.

52. The electrode as specified in Claim 51, wherein said second portion and said third portion are different materials.

53. The electrode as specified in Claim 52, wherein said first portion and said third portion are different materials.

54. The dynamic random access memory device as specified in Claim 51, further comprising:

a) a dielectric layer overlying said third portion; and

b) a cell plate electrode overlying said dielectric layer.

55. The dynamic random access memory device as specified in Claim 51 further comprising a transistor.

56. An electrode, comprising:

a) a contact formed in an insulative layer;

b) a diffusion barrier portion overlying said contact, said insulative layer surrounding a sidewall of said diffusion barrier portion; and

c) an oxidation resistant portion overlying said diffusion barrier portion and extending above an upper surface of said insulative layer, said diffusion barrier portion configured to inhibit diffusion of atoms between said contact and said oxidation resistant portion.

57. The electrode as specified in Claim 56, further comprising a reducing contact resistance portion interposed between said contact and said diffusion barrier portion, said reducing contact resistance portion configured to reduce a contact resistance between said contact and said diffusion barrier portion.

58. A method for fabricating an electrode, comprising the following steps:

a) forming an insulative layer;

b) forming an opening in the insulative layer;

c) forming a first portion of the electrode in a lower region of the opening;

d) forming a second portion of the electrode in the opening and overlying the first portion, said insulative layer encompassing a sidewall of said second portion; and

e) forming a third portion of the electrode overlying the second portion and overlying at least a portion of the insulative layer, wherein said first portion and said second portion are different materials.

59. The electrode as specified in Claim 58, wherein said second portion and said third portion are different materials.

60. The electrode as specified in Claim 59, wherein said first portion and said third portion are different materials.

61. A method for fabricating an electrode, comprising the following steps:

a) forming an insulative layer;

b) forming an opening in the insulative layer;

c) forming a first portion of the electrode in a lower region of the opening;

d) forming a second portion of the electrode in the opening and overlying the first

portion, said insulative layer encompassing a sidewall of said second portion; and

e) forming a third portion of the electrode overlying the second portion and extending above a top surface of the insulative layer, wherein said first portion and said second portion are different materials.

62. The electrode as specified in Claim 61, wherein said second portion and said third portion are different materials.

63. The electrode as specified in Claim 62, wherein said first portion and said third portion are different materials.

64. The method as specified in Claim 61, further comprising the step of encompassing a lower sidewall of the third portion with said insulative layer.

65. The method as specified in Claim 61, further comprising the step of forming a fourth portion underlying the second portion and overlying the first portion.

66. The method as specified in Claim 61, wherein said step of forming said insulative layer comprises the following steps:

a) depositing a first portion of said insulative layer to overlie said substrate; and

b) depositing a second portion of said insulative layer to overlie said first portion of said insulative layer, said second portion of said insulative layer having oxidation

resistant properties.

67. The method as specified in Claim 66, further comprising the following steps:

a) patterning said second portion of said insulative layer to define the opening; and

b) removing exposed regions of said first and second portions of said insulative layer to create the opening.

68. The method as specified in Claim 66, further comprising the step of planarizing said first portion of said insulative layer.

69. A method for fabricating an electrode, comprising the following steps:

a) forming a recess in an electrically insulative layer to expose a substrate;

b) forming a contact in the recess overlying and in electrical contact with the substrate;

c) forming a diffusion barrier layer in the recess and overlying the contact;

d) forming a conductive oxidation resistant layer in the recess and overlying the diffusion barrier layer;

e) removing portions of the conductive oxidation resistant layer lying outside of the recess; and

f) removing portions of the insulative layer to expose an upper sidewall of said conductive oxidation resistant layer, said diffusion barrier layer inhibiting diffusion of

atoms between said contact and said conductive oxidation resistant layer.

70. The method as specified in Claim 69, further comprising the step of forming a reducing contact resistance layer interposed between said contact and said diffusion barrier layer, said reducing contact resistance layer configured to reduce a contact resistance between said contact and said diffusion barrier layer.

71. The method as specified in Claim 69, further comprising the following steps:

a) forming a further electrically insulative region in the recess to overlie the conductive oxidation resistant layer; and

b) removing the further electrically insulative region in the recess during said step of removing portions of the insulative layer to expose the conductive oxidation resistant layer in the recess.

72. The method as specified in Claim 69, wherein said step of removing portions of the conductive oxidation resistant layer comprises planarizing the conductive oxidation resistant layer.

73. The method as specified in Claim 69, further comprising the following steps:

a) forming a dielectric layer overlying the conductive oxidation resistant layer; and

b) forming a cell plate layer overlying the dielectric layer.

74. A method for fabricating a capacitor, comprising the following steps:

a) forming an electrically insulative layer overlying a substrate;

b) forming an opening in said insulative layer in order to expose said substrate;

c) forming a conductive plug in said opening, said conductive plug forming a first portion of a first electrode of said capacitor;

d) providing a recess in said opening between a surface of said insulative layer and a surface of said conductive plug;

e) forming a diffusion barrier layer in said recess such that a sidewall of said diffusion barrier layer is surrounded by said insulative layer, said diffusion barrier layer overlying said conductive plug and forming a second portion of said first electrode;

f) forming a conductive oxidation resistant layer overlying said insulative layer and in the recess overlying said diffusion barrier layer, said diffusion barrier layer configured to inhibit diffusion of atoms between said conductive plug and said conductive oxidation resistant layer;

g) removing portions of the conductive oxidation resistant layer overlying said insulative layer while retaining portions of said conductive oxidation resistant layer in the recess, remaining portions of the conductive oxidation resistant layer forming a third portion of said first electrode;

h) removing portions of said insulative layer to expose an upper portion of a sidewall of said conductive oxidation resistant layer;

i) retaining a portion of said insulative layer at a lower portion of said sidewall of

said conductive oxidation resistant layer;

j) forming a dielectric layer overlying said conductive oxidation resistant layer; and

k) forming a second electrode overlying said dielectric layer, said first and said second electrodes and said dielectric layer forming the capacitor.

75. The method as specified in Claim 74, wherein said step of forming said insulative layer comprises the following steps:

a) depositing a first portion of said insulative layer to overlie said substrate; and

b) depositing a second portion of said insulative layer to overlie said first portion of said insulative layer, said second portion of said insulative layer having oxidation resistant properties.

76. The method as specified in Claim 75, further comprising the following steps:

a) patterning said second portion of said insulative layer to define the opening; and

b) removing exposed regions of said first and second portions of said insulative layer to create the opening.

77. The method as specified in Claim 76, further comprising the step of planarizing said first portion of said insulative layer.

78. The method as specified in Claim 74, further comprising the steps of:

a) depositing a further insulative layer in said recess to overlie at least a portion of said conductive oxidation resistant layer; and

b) removing said further insulative layer during said step of removing portions of said insulative layer.

79. The method as specified in Claim 74, further comprising the step of forming a reducing contact resistance layer interposed between said conductive plug and said diffusion barrier layer, said reducing contact resistance layer configured to reduce a contact resistance between said contact and said diffusion barrier layer.

80. A method for fabricating an electrode, comprising the following steps:

a) forming an electrically insulative layer overlying a substrate;

b) masking the insulative layer to define a future opening in the insulative layer;

c) etching the insulative layer in an exposed region to form the opening and to expose the substrate;

d) forming a contact to the substrate in the opening;

e) recessing a top surface of the contact from a surface of the insulative layer;

f) forming a diffusion barrier layer overlying the contact;

g) removing portions of the diffusion barrier layer overlying the insulative

layer;

h) forming a conductive oxidation resistant layer overlying the diffusion barrier layer;

i) removing portions of the conductive oxidation resistant layer overlying the insulative layer; and

j) removing upper portions of the insulative layer to expose an upper sidewall of the conductive oxidation resistant layer, wherein said conductive oxidation resistant layer, said diffusion barrier layer, and said contact form the electrode.

81. The method as specified in Claim 80, wherein said step of forming an electrically insulative layer comprises the following steps:

a) depositing a first portion of said insulative layer to overlie said substrate; and

b) depositing a second portion of said insulative layer to overlie said first portion of said insulative layer, said second portion of said insulative layer having oxidation resistant properties.

82. The method as specified in Claim 80, further comprising the following steps:

a) creating a dielectric layer overlying the conductive oxidation resistant layer; and

b) creating a further electrode overlying the dielectric layer.

83. The method as specified in claim 80, further comprising forming a reducing contact resistance region interposed between the contact and the diffusion barrier layer, said reducing contact resistance region configured to reduce a contact resistance between said contact and the diffusion barrier layer.

84. A method for fabricating an electrode, comprising the following steps:

a) forming a contact overlying and in electrical contact with a substrate;

b) interposing a diffusion barrier layer between the contact and a conductive oxidation resistant layer, at least said diffusion barrier layer and said conductive oxidation resistant layer forming an electrode of said capacitor;

c) encompassing a sidewall of said diffusion barrier layer with an insulative layer, said insulative layer prohibited from overlying and underlying said diffusion barrier layer; and

d) encompassing a bottom portion of a sidewall of said conductive oxidation resistant layer with the insulative layer, a top portion of the sidewall extending above the insulative layer.

85. The method as specified in Claim 84, further comprising the following steps:

a) forming a dielectric layer overlying said conductive oxidation resistant layer;

b) applying a temperature capable of oxidizing said diffusion barrier layer;

c) preventing oxidation of said diffusion barrier layer during said step of applying; and

d) forming a further electrode overlying said dielectric layer.

86. The method as specified in Claim 85, further comprising:

a) forming a plurality of the capacitors; and

b) providing electrical communication between said further electrodes of said plurality.

87. The method as specified in Claim 84, further comprising the following steps:

a) depositing said insulative layer to overlie said substrate prior to said step of forming the contact;

b) patterning said insulative layer to define a future opening; and

c) removing a portion of said insulative layer to create the opening in said insulative layer in which to form the contact.

88. The method as specified in Claim 84, further comprising forming a reducing contact resistance region interposed between the contact and the diffusion barrier layer, said reducing contact resistance region configured to reduce a contact resistance between said contact and the diffusion barrier layer.---.

In the drawings:

Please insert additional figures 12-28, submitted herewith, into the patent application.

Respectfully submitted,

Susan B. Collier
Agent for the Applicant
Registration No. 34,566
(208)368-4514

SC/lab

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express mail in an envelope addressed to: Commissioner of Patents & Trademarks, Washington, D.C. 20231, on December 14, 1995.

December 14, 1995.
Susan B. Collier, Agent of Record

0S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pierre C. Fazan et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.434US2
Title:	METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS	

SUPPLEMENTAL PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

After entering the Preliminary Amendment also enclosed herewith, please further amend the application as follows:

IN THE SPECIFICATION

On page 2, line 1, before "This invention pertains", please insert the sentence, --This application is a divisional of U.S Serial No. 08/572,392 filed 12/14/95 which is a continuation of U.S. Serial No. 08/390,336 filed 02/17/95--.

IN THE CLAIMS

Please cancel claims 58-68 without prejudice or disclaimer, and amend the remaining claims as follows:

28. (Amended) An electrode[,] comprising:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said insulative layer, wherein said first portion and said second portion are different materials.

31. (Amended) An dynamic random access memory device[,] comprising:

an electrode which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said insulative layer, wherein said first portion and said second portion are different materials.

34. (Amended) An dynamic random access memory device[,] comprising:

a capacitor which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said insulative layer, wherein said first portion and said second portion are different materials.

39. (Amended) An electrode[,] comprising:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are different materials.

48. (Amended) A dynamic random access memory device(,) comprising:

an electrode which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are different materials.

51. (Amended) A dynamic random access memory device[,] comprising:

a capacitor which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are different materials.

56. (Amended) An electrode[,] comprising:

a) a contact formed in an insulative layer;

b) a diffusion barrier portion overlying said contact, said insulative layer surrounding a sidewall of said diffusion barrier portion; and

c) an oxidation resistant portion overlying said diffusion barrier portion and extending above an upper surface of said insulative layer, said diffusion barrier portion configured to inhibit diffusion of atoms between said contact and said oxidation resistant portion.

80. (Amended) A method for fabricating an electrode, comprising [the following steps]:

a) forming an electrically insulative layer overlying a substrate;

b) masking the insulative layer to define a future opening in the insulative layer;

c) etching the insulative layer in an exposed region to form the opening and to expose the substrate;

d) forming a contact to the substrate in the opening;

e) recessing a top surface of the contact from a surface of the insulative layer;

f) forming a diffusion barrier layer overlying the contact;

g) removing portions of the diffusion barrier layer overlying the insulative layer;

h) forming a conductive oxidation resistant layer overlying the diffusion barrier layer;

i) removing portions of the conductive oxidation resistant layer overlying the insulative layer; and

j) removing upper portions of the insulative layer to expose an upper sidewall of the conductive oxidation resistant layer, wherein said conductive oxidation resistant layer, said diffusion barrier layer, and said contact form the electrode.

81. (Amended) The method as specified in Claim 80, [where said step of] wherein forming an electrically insulative layer comprises [the following steps]:

a) depositing a first portion of said insulative layer to overlie said substrate; and

b) depositing a second portion of said insulative layer to overlie said first portion of said insulative layer, said second portion of said insulative layer having oxidation resistant properties.

82. (Amended) The method as specified in Claim 80, further comprising [the following steps]:

a) creating a dielectric layer overlying the conductive oxidation resistant layer; and

b) creating a further electrode overlying the dielectric layer.

84. (Amended) The method for fabricating an electrode, comprising [the following steps]:

a) forming a contact overlying and in electrical contact with a substrate;

b) interposing a diffusion barrier layer between the contact and a conductive oxidation resistant layer, at least said diffusion barrier layer and said conductive oxidation resistant layer forming an electrode of said capacitor;

c) encompassing a sidewall of said diffusion barrier layer with an insulative layer, said insulative layer prohibited from overlying and underlying said diffusion barrier layer; and

d) encompassing a bottom portion of a sidewall of said conductive oxidation

resistant layer with the insulative layer, a top portion of the sidewall extending above the insulative layer.

85. (Amended) The method as specified in Claim 84, further comprising [the following steps]:

a) forming a dielectric layer overlying said conductive oxidation resistant layer;

b) applying a temperature capable of oxidizing said diffusion barrier layer;

c) preventing oxidation of said diffusion barrier layer during said [step of] applying; and

d) forming a further electrode overlying said dielectric layer.

87. (Amended) The method as specified in Claim 84, further comprising [the following steps]:

a) depositing said insulative layer to overlie said substrate prior to said [step of] forming the contact;

b) patterning said insulative layer to define a future opening; and

c) removing a portion of said insulative layer to create the opening in said insulative layer in which to form the contact.

REMARKS

With this amendment, applicant cancels claims 58-68, and amends claims 28, 31, 34, 39, 48, 51, 56, 80-82, 84-85 and 87 were amended to remove "step" language and thus to clarify applicant's intent that these claims not be construed under 35 U.S.C. 112, paragraph six. Unless explicitly noted, none of the claims are intended to be construed under this paragraph.

The Examiner is invited to call the undersigned attorney with any questions or concerns arising during the examination.

Respectfully submitted,
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Date 24 Jan. 2000 By _____
Eduardo E. Drake
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Shawn L. Hise _____
Name Signature

A METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS

Field of the Invention:

This invention pertains to semiconductor technology, and more particularly to storage cell capacitors for use in dynamic random access memories.

Background of the Invention:

As memory devices become more dense it is necessary to decrease the size of circuit components. One way to retain the storage capacity of a dynamic random access memory (DRAM) device and decrease its size is to increase the dielectric constant of the dielectric layer of the storage cell capacitor. In order to achieve the charge storage efficiency needed in 256 megabit(Mb) memories and above, materials having a high dielectric constant, typically greater than 50, can be used as the dielectric layer to insulate the storage node electrode and cell plate electrode of the storage cell capacitor one from the other. A dielectric constant is a value characteristic of a material and is proportional to the amount of charge that can be stored in the material when it is interposed between two electrodes. $Ba_xSr_{(1-x)}TiO_3$ [BST], $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$ [PZT], $(Pb,La)(Zr,Ti)O_3$ [PLZT], $(Pb,La)TiO_3$ [PLT], KNO_3, and $LiNbO_3$ are among some of the high dielectric constant materials that can be used in this application. These materials have dielectric constant values

above 50 and will likely replace the standard Si_3N_4, SiO_2/Si_3N_4, Si_3N_4/SiO_2, or $SiO_2/Si_3N_4/SiO_2$ composite films used in 256 kilobits (Kb) to 64 megabits (Mb) generations of DRAMs. Si_3N_4 and SiO_2/Si_3N_4 composite films have dielectric constant values of 7 or less. The storage node and cell plate electrodes are also referred to as first and second electrodes.

Unfortunately BST is incompatible with existing processes and can not be simply deposited on a polysilicon electrode as was the case for the lower dielectric constant materials, such as Si_3N_4 and SiO_2/Si_3N_4 composite layers. In the storage cell capacitor incorporating BST, described in the IDEM-91 article entitled, A STACKED CAPACITOR WITH $(Ba_xSr_{1-x})TiO_3$ FOR 256M DRAM by Koyama et al., the storage node electrode typically comprises a layer of platinum overlying a tantalum layer which, in turn, overlies a polysilicon plug. Platinum is used as the upper portion of the first electrode since it will not oxidize during a BST deposition or subsequent anneal. An electrode that oxidizes would have a low dielectric constant film below the BST, thereby negating the advantages provided by the high dielectric constant material. The tantalum layer is introduced to avoid Si and Pt inter-diffusion and to prevent the formation of SiO_2 on top of the platinum surface. In addition, the platinum protects the top surface of the tantalum from strong oxidizing conditions during the BST deposition. Figure 1 depicts the stacked storage node electrode comprising tantalum 1, platinum 2 (Ta/Pt) overlying the polysilicon plug 3.

However, the sidewalls 4 of the tantalum 1 formed during this process are subject to oxidation during the subsequent deposition of the BST layer. Since the tantalum 1 oxidizes the polysilicon plug 3 is also susceptible to oxidation. When portions of the polysilicon plug 3 and tantalum 1 are consumed by oxidation the capacitance of the storage cell capacitor is decreased since the storage node electrode is partially covered by a low dielectric constant film. Therefore the memory device cannot be made as dense. In addition, the storage node contact resistance increases drastically.

Objects of the Invention:

An object of the invention is to increase density of a memory device by increasing capacitance of storage cell capacitors. The storage cell capacitor of the invention features a storage node electrode having a barrier layer of tantalum or another material which experiences no oxidation during the formation of the storage cell capacitor. The barrier layer is interposed between a conductive plug and a non-oxidizing conductive material such as platinum. A dielectric layer, typically $Ba_xSr_{(1-x)}TiO_3$ [BST], is deposited on the non-oxidizing material. The barrier layer is surrounded on its sides by an insulative layer.

The insulative layer protects the barrier layer from oxidizing during the deposition and anneal of the BST thereby also eliminating oxidization of the conductive plug. By

eliminating oxidization of the barrier layer and the conductive plug capacitance is maximized.

Summary of the Invention:

The invention is a storage node capacitor having a storage node electrode comprising a barrier layer interposed between a conductive plug and an oxidation resistant conductive layer and the method for fabricating the same. A thick insulative layer protects the sidewalls of the barrier layer during the deposition and anneal of a dielectric layer having a high dielectric constant.

The method comprises forming the conductive plug in a thick layer of insulative material such as oxide or oxide/nitride. The conductive plug is recessed from a planarized top surface of the thick insulative layer. The barrier layer is formed in the recess. The process is then continued with a formation of an oxidation resistant conductive layer and the patterning thereof to complete the formation of the storage node electrode.

Next a dielectric layer having a high dielectric constant is formed to overly the storage node electrode and a cell plate electrode is then fabricated to overly the dielectric layer.

Since the barrier layer is protected during the formation of the dielectric layer by both the oxidation resistant

conductive layer and the thick insulative layer there is no oxidation of the barrier layer or the contact plug thereby maximizing capacitance of the storage node and reducing high contact resistance issues.

Brief Description of the Drawings:

Figure 1 is a cross-sectional view of a portion of a partially processed semiconductor wafer of the related art.

Figures 2-11 are cross-sectional views of a portion of a partially processed semiconductor wafer depicting the steps of the invention for fabricating a storage cell capacitor.

Figure 2 depicts field-effect transistors overlying a silicon substrate and wordlines overlying field oxide.

Figure 3 is the wafer portion of Figure 2 following the deposit of an undoped thick oxide layer and planarization thereof.

Figure 4 is the wafer portion of Figure 3 following the masking and subsequent etching of the deposited oxide layer to form self-aligned openings.

Figure 5 is the wafer portion of Figure 4 following the formation of polysilicon plugs in the openings and the removal of the mask shown in Figure 4.

Figure 6 is the wafer portion of Figure 5 following the recessing of the polysilicon plug in the thick oxide layer.

Figures 7a and 7b are wafer portions of Figure 6 following the deposition of a tantalum layer.

Figures 8a and 8b are wafer portions of Figures 7a and 7b following the planarization of the tantalum layer.

Figures 9a and 9b are wafer portions of Figures 8a and 8b following the deposition of a platinum layer.

Figures 10a and 10b are the wafer portions of Figure 9a and 9b following the etching of the platinum layer to complete the formation of the storage node.

Figures 11a and 11b are wafer portions of Figures 10a and 10b following the deposition of a BST dielectric layer and a cell plate layer and patterning of these layers to complete the formation of the storage cell capacitor.

Detailed Description of the Preferred Embodiment:

The method for fabricating the storage cell capacitor of the invention is shown pictorially in Figures 2-11.

Referring to Figure 2, a cross-sectional view of an in-process dynamic random access memory (DRAM) cell is shown following conventional local oxidation of silicon (LOCOS) or

special LOCOS processing which creates substantially planar field oxide regions 5 (created using modified LOCOS or trench isolation processes) and future active areas 6 (those regions of the substrate not covered by field oxide) on a silicon substrate 7. The creation of the field oxide is preceded or followed by a thermally grown dielectric layer 8 of silicon oxide. The depicted cell is one of many cells that are fabricated simultaneously and comprise a memory array. Following the creation of the field oxide region 5 and dielectric layer 8 a first conductively doped polysilicon layer 10, a metal silicide layer (Wsi_x) 15, an oxide layer 16, and a thick nitride layer 20 are deposited. The thick nitride layer 20 will function as an etch stop during the storage node buried contact etch, thus allowing self-alignment if desired. The layers are patterned and etched to form wordlines 21 and N-channel (NCH) field effect transistors 22. The polysilicon layer 10 forms the gate regions of the FETs and is insulated from lightly-doped source/drain regions 25 by the dielectric layer 8. The lightly-doped regions 25 are created utilizing a phosphorus or arsenic implant. Deposition, densification and a reactive ion etch (RIE) of a silicon nitride spacer layer has created principal spacers 35 which offset an arsenic implant used to create the heavily-doped source/drain regions 30. Principal spacers 35 insulate the wordlines and FETs from subsequent digit line and capacitor fabrications. Eventually the wordlines are connected to periphery contacts. The periphery contacts are located at the end of the array and are capable of being in electrical communication with peripheral circuitry.

The formation of the FETs 22 and wordlines 21 as described are exemplary of one application to be used in conjunction with the present embodiment of the invention. Other methods of fabrication and other applications are also feasible and perhaps equally viable.

In Figure 3 a thick insulative conformal layer of undoped oxide 40 is blanket deposited to fill the storage node areas and overlie the FETS 22 and wordlines 21. The oxide is undoped to minimize dopant out diffusion from the oxide 40 to the doped regions of the substrate. The oxide is planarized, preferably chemical mechanically planarized (CMP), in order to provide a uniform height. Optionally nitride, oxynitride or another suitable material may be deposited as the insulative layer.

At this juncture buried digit lines may be fabricated as described in U.S. patent number 5,168,073 herein incorporated by reference. In the case where the buried digit lines are formed by the method described in U.S. patent 5,168,073 the oxide 40 is deposited in two steps, one deposit prior to the digit line formation and one deposit subsequent to the digit line formation. In this case, an initial thick oxide layer is deposited and planarized and then overlaid with a relatively thick Si_3N_4 layer. The Si_3N_4 layer is then planarized. When the thick insulative layer is comprised only of oxide it is possible for oxygen to diffuse through the oxide. By overlying the oxide with Si_3N_4 it is possible to prohibit oxygen diffusion though the oxide.

Referring to Figure 4, mask 53 defines self-aligned substrate contact area 55. The oxide 40 is etched to form a self-aligned openings 50 exposing the contact areas 55 of the substrate 7.

Referring to Figure 5, in order to provide electrical communication between the substrate 7 and the storage cell capacitor a polysilicon plug 65 is formed in each opening 50. The actual method used to form the polysilicon plugs 65 is not critical, two options being a selective silicon growth from the contact area 55 or a doped polysilicon deposition and subsequent etch back or CMP back.

Referring now to Figure 6, an upper portion of the polysilicon plugs 65 is removed during a dry etch in order to form a recesses 70, Typically, this etch back is 50 to 400 nano meters (nm). In a case where the polysilicon plugs 65 are formed during a selective silicon growth it is possible to form the recess 70 by controlling the growth.

Referring to Figure 7a, a tantalum layer 75, with a thickness larger than the depth of the recesses 70, is formed by a chemical vapor deposition (CVD) or a sputtering process performed at room temperature. The tantalum layer 75 provides a barrier against silicon diffusion of the polysilicon plug during subsequent high temperature anneals and other materials capable of prohibiting silicon diffusion may be used in place of tantalum. For example, titanium and titanium nitride may be used as well as other materials. Alternately, a tantalum layer 75 may be formed wherein the thickness is less than or

equal to the depth of the recess. Figure 7b depicts the latter case. In this particular case the storage cell capacitor gains more vertical area thereby increasing capacitance.

Referring to Figures 8a and 8b, the tantalum layer 75 of Figures 7a and 7b, respectively, is planarized, preferably by CMP, in order to expose at least the oxide layer 40 and in order to retain tantalum 75 in recesses 70 overlying the polysilicon plugs 65. Portions of the oxide layer 40 may be planarized during this step. It is important, of course to retain a sufficient depth of tantalum 75 in order to inhibit silicon diffusion of the polysilicon plugs 65. It can be seen that only the upper surface of the tantalum layer 75 is exposed and that the tantalum sidewalls 80 are protected by the oxide layer 40.

Referring to Figures 9a and 9b a platinum layer 85 is formed by CVD or a sputtering technique. The platinum layer 85 overlies the tantalum layer 75 shown in Figures 8a and 8b, respectively. Since the platinum layer 85 is resistant to oxidation it provides an excellent surface for the deposition of the high dielectric constant material. Other materials which are resistant to oxidation may be used in place of the platinum. For example, RuO_2 and TiN, as well as other non-oxidizing materials may be used. Since the tantalum layer is recessed below the oxide layer 40, a thick layer of platinum may be deposited without decreasing the density of the device. By using very thick platinum electrodes, the capacitance area is increased by the sidewall area contribution. Therefore,

the platinum is deposited from at least a thickness of 50nm to a thickness of 1 micro meter(μm).

Figures 10a and 10b depict the structure following the masking of the platinum layer 85 overlying the tantalum and the removal of unmasked portions of the platinum layer 85 to form the completed storage node electrode of the storage cell capacitor. Typically the storage node electrode is thought of as comprising the tantalum layer 75 and the platinum layer 85. The polysilicon plug 65 is often thought of as an electrical interconnect interposed between the substrate and the storage node electrode, although it can be thought of as a portion of the storage node itself.

Figures 11a and 11b depict the storage cell capacitor following a deposition and anneal of a dielectric layer 90 overlying the platinum layer 85 of Figures 10a and 10b, respectively. The dielectric layer is typified as having a high dielectric constant. The storage cell capacitor fabrication is completed with the sputter or CVD of a 50 to 200nm thick cell plate layer 95 to form a cell plate electrode. The cell plate layer 95 is typically Platinum, TiN or some other conductive material.

Among the suitable materials for a dielectric layer having a high dielectric constant are $Ba_xSr_{(1-x)}TiO_3$ [BST], $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$ [PZT], $(Pb,La)(Zr,Ti)O_3$ [PLZT], $(Pb,La)TiO_3$ [PLT], KNO_3, and $LiNbO_3$. In the applicant's invention BST is the preferred material and is deposited at a thickness range of 30nm-300nm by RF-magnetron

sputtering or CVD. The tantalum layer 75 is not oxidized during the application of a high temperature anneal due to the fact that it is protected on its sidewalls 80 by the oxide layer 40 and that it is protected on its upper surface by the platinum layer 85, see Figure 11. Therefore even after the formation of the dielectric layer the recess retains the original tantalum 75 formed therein and capacitance is not sacrificed as it would be when portions of the tantalum 75 are consumed by oxidation. Therefore capacitance is effectively increased over methods where portions of tantalum are oxidized.

The process can be continued or modified to accommodate the steps described in U.S. patent 5,168,073, previously incorporated by reference, for providing electrical interconnection between a plurality of capacitors thus formed.

By utilizing the method of the preferred embodiments of the invention, a high density memory device is provided featuring a stacked capacitor formed in a compact area as a result of a dielectric layer having a high dielectric constant and retention of storage node integrity during an anneal of the dielectric layer and the capability of depositing a very thick platinum layer as a portion of the first electrode.

Although a process and an alternate process have been described for forming the storage cell capacitor it is apparent the process is equally applicable for the fabrication of other types of capacitors used in integrated circuits. It should also be apparent to one skilled in the art that changes

and modifications, such as deposition depths, may be made thereto without departing from the spirit and scope of the invention as claimed.

What is Claimed is:

1. A method for fabricating a capacitor for an integrated circuit, comprising the following steps:

a) interposing a diffusion barrier layer between a substrate contact and a conductive oxidation resistant layer, at least said diffusion barrier layer and said conductive oxidation resistant layer forming a first electrode of said capacitor; and

b) encompassing sidewalls of said diffusion barrier layer with an insulative layer, said insulating layer prohibited from overlying and underlying said diffusion barrier layer.

2. The method as specified in Claim 1, further comprising the following steps:

a) depositing a dielectric layer overlying said conductive oxidation resistant layer;

b) performing a high temperature anneal;

c) preventing oxidation of said barrier layer during said step of performing; and

d) depositing a second electrode overlying said dielectric layer, said dielectric layer electrically insulating said first and said second electrodes one from the other.

3. The method as specified in Claim 2, further comprising:

a) forming a plurality of said capacitors having said first and said second electrodes; and

b) providing electrical communication between said second electrodes of said plurality.

4. The method as specified in Claim 1, wherein said step of encompassing said sidewalls comprises depositing said insulative layer to overly said substrate, wherein said

insulative layer is selected from a group of insulative materials comprising oxide, nitride and oxynitride.

5. The method as specified in Claim 1, wherein said step of encompassing said sidewalls comprises:

a) depositing a first portion of said insulative layer to overly said substrate; and

b) depositing a second portion of said insulative layer to overly said first portion, said second portion having oxidation resistant properties.

6. The method as specified in Claim 5, further comprising planarizing said first portion.

7. A method for forming a capacitor, comprising the following steps:

a) forming a first capacitor electrode overlying a substrate contact;

b) forming a dielectric layer overlying said first electrode;

c) performing a high temperature anneal;

d) preventing oxidation of said first electrode during said high temperature anneal; and

e) forming a second electrode, wherein said dielectric layer electrically insulates said first and said second electrodes.

8. The method as specified in Claim 7, further comprising increasing a capacitance of said capacitor by selecting said dielectric material from a group of materials having a dielectric constant greater than 50, wherein said group comprises $Ba_xSr_{(1-x)}TiO_3$, $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$, $(Pb,La)(Zr,Ti)O_3$, $(Pb,La)TiO_3$, KNO_3, and $LiNbO_3$.

9. A method for fabricating a capacitor, comprising the following steps:

a) depositing a thick insulative layer overlying a substrate;

b) forming an opening in said insulative layer in order to expose said substrate;

c) forming a conductive plug in said opening, said conductive plug forming a first portion of a first electrode of said capacitor;

d) providing a recess in said opening between a surface of said insulative layer and a surface of said conductive plug;

e) forming a conductive barrier layer, for preventing diffusion, in said recess such that said barrier layer is surrounded on sidewalls by said insulative layer, said barrier layer overlying said conductive plug and forming a second portion of said first electrode;

f) forming a conductive oxidation resistant layer overlying said barrier layer to form a third portion of said first electrode;

g) forming a dielectric layer overlying said oxidation resistant layer; and

h) forming a second electrode overlying said dielectric layer, said dielectric layer electrically insulating said first and said second electrodes one from the other.

10. The method as specified in Claim 9, wherein said step of forming said dielectric layer comprises the following steps:

a) applying temperatures capable of oxidizing said barrier layer; and

b) preventing said barrier layer from oxidizing during said step of applying.

11. The method as specified in Claim 9, further comprising the step of planarizing said insulative layer prior to forming said conductive plug.

12. The method as specified in Claim 9, wherein said step of forming said conductive plug comprises depositing polysilicon to fill said opening.

13. The method as specified in Claim 12, wherein said step of providing said recess comprises etching back a portion of said polysilicon to create said recess in said thick insulative layer.

14. The method as specified in Claim 12, wherein said step of forming said conductive plug comprises planarizing said polysilicon to expose said insulative layer.

15. The method as specified in Claim 14, further comprising the step of performing a chemical mechanical planarization to effect said step of planarizing.

16. The method as specified in Claim 12, wherein said step of forming said conductive plug comprises etching back said polysilicon to expose said insulative layer.

17. The method as specified in Claim 9, wherein said step of forming said conductive plug comprises selectively growing silicon in said opening.

18. The method as specified in Claim 17, wherein said step of providing said recess comprises prohibiting said step of selectively growing silicon in said recess.

19. The method as specified in Claim 9, wherein said step of forming said thick insulative layer comprises the following steps:

a) depositing a first portion of said insulative layer to overly the substrate; and

b) depositing a second portion of said insulative layer to overly said first portion, said second portion capable of prohibiting oxygen penetration.

20. The method as specified in Claim 9, wherein the step of forming said dielectric layer comprises forming said dielectric layer with a material typified as having a high dielectric constant.

21. The method as specified in Claim 9, wherein the step of forming said barrier layer comprises forming said barrier layer with tantalum.

22. The method as specified in Claim 9, wherein the step of forming said oxidation resistant layer comprises forming said oxidation resistant layer with platinum.

23. The method as specified in Claim 9, wherein the step of forming a barrier layer comprises:

a) sputtering tantalum to overly said conductive plug and said thick insulation layer; and

b) removing portions of said tantalum to exposes said thick insulative layer while retaining said tantalum in said recess.

24. The method as specified in Claim 23, wherein said step of removing comprises performing a chemical mechanical planarization.

25. The method as specified in Claim 9, wherein said step of forming said second electrode comprises sputtering platinum to overly said dielectric layer.

26. The method as specified in Claim 9, wherein said step of forming said dielectric layer comprises depositing by chemical

vapor deposition a high dielectric material from the group of materials comprising $Ba_xSr_{(1-x)}TiO_3$, $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$, $(Pb,La)(Zr,Ti)O_3$, $(Pb,La)TiO_3$, KNO_3, and $LiNbO_3$.

27. The method as specified in Claim 9, wherein the step of depositing said thick insulative layer comprises depositing a material selected from the group comprising oxide, nitride, and oxynitride.

Serial No.:
Inventor(s): Fazan et al

A METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS

ABSTRACT

The invention is a storage cell capacitor having a storage node electrode comprising a barrier layer interposed between a conductive plug and an oxidation resistant layer. A thick insulative layer protects the sidewalls of the barrier layer during the deposition and anneal of a dielectric layer having a high dielectric constant.

The method comprises forming the conductive plug in a thick layer of insulative material such as oxide or oxide/nitride. The conductive plug is recessed from a planarized top surface of the thick insulative layer. The barrier layer is formed in the recess. The process is then continued with a formation of an oxidation resistant conductive layer and the patterning thereof to complete the formation of the storage node electrode.

Next a dielectric layer having a high dielectric constant is formed to overly the storage node electrode and a cell plate electrode is fabricated to overly the dielectric layer.

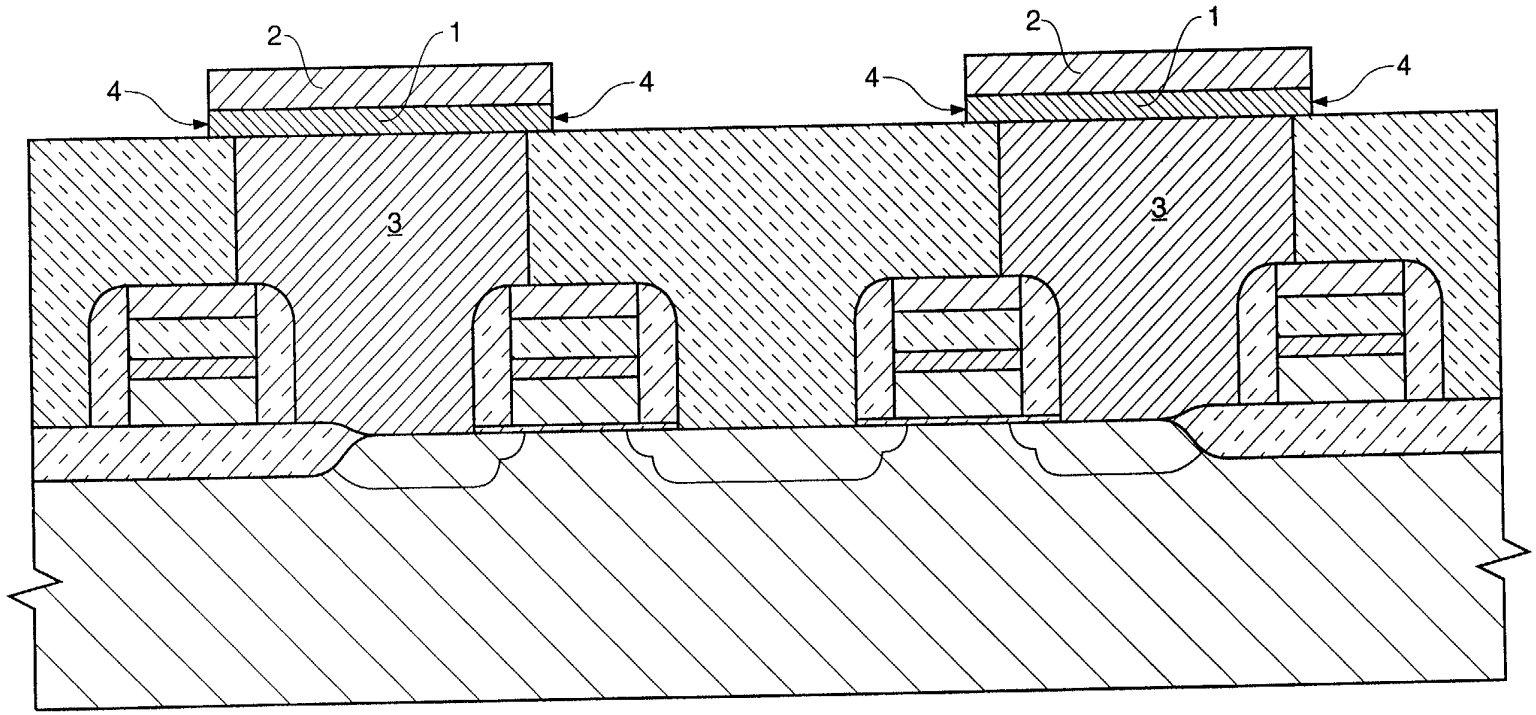

FIG. 1
(RELATED ART)

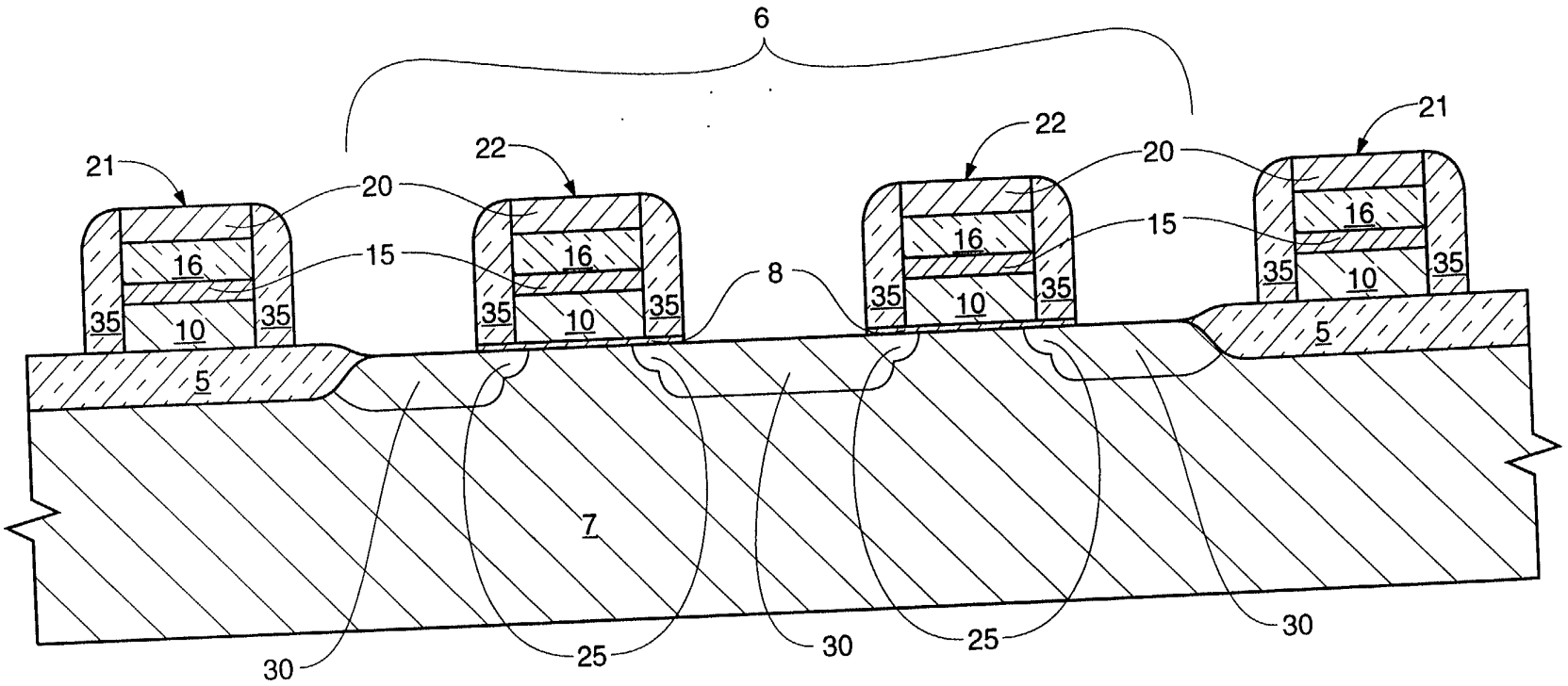

FIG. 2

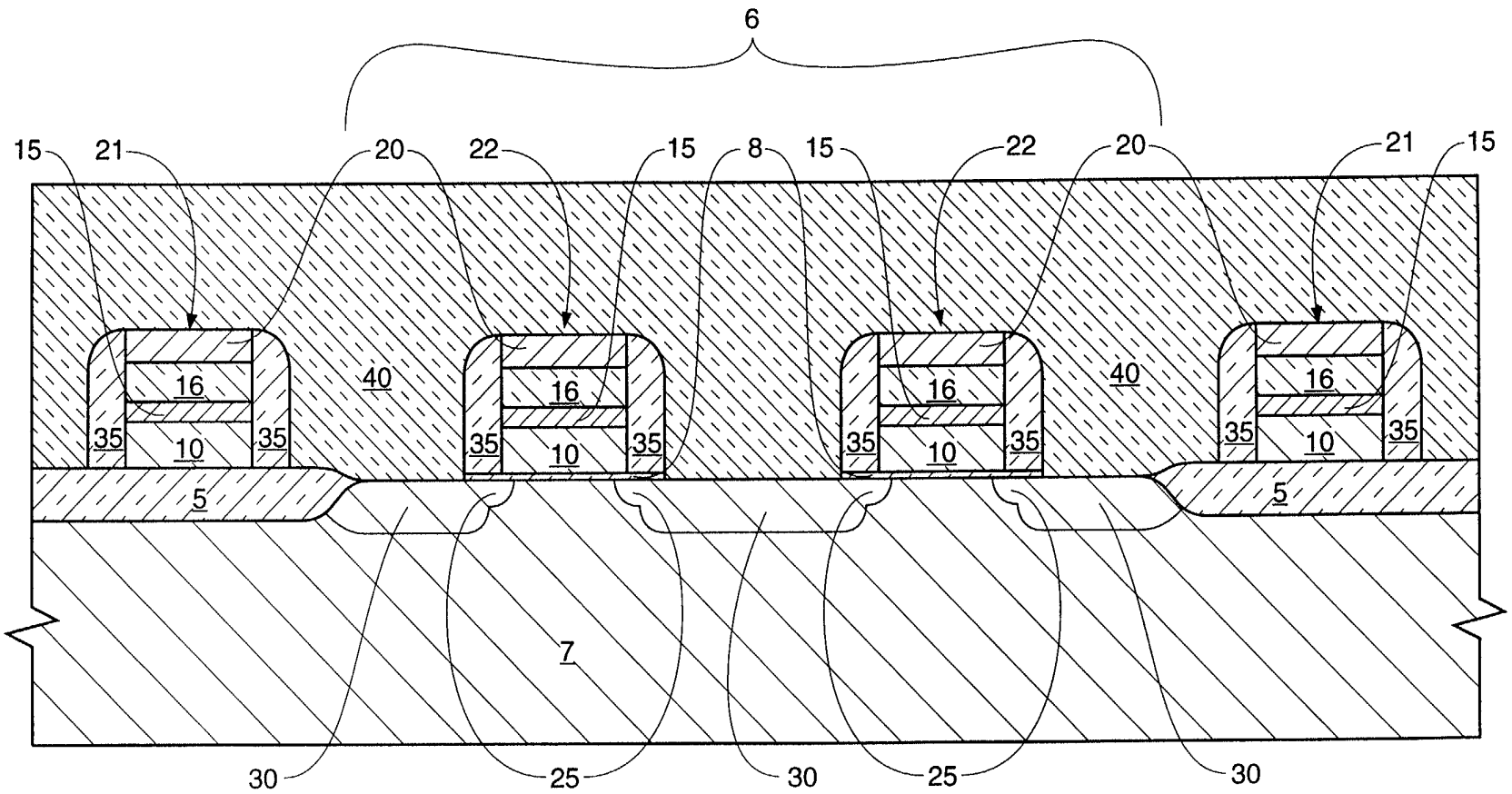

FIG. 3

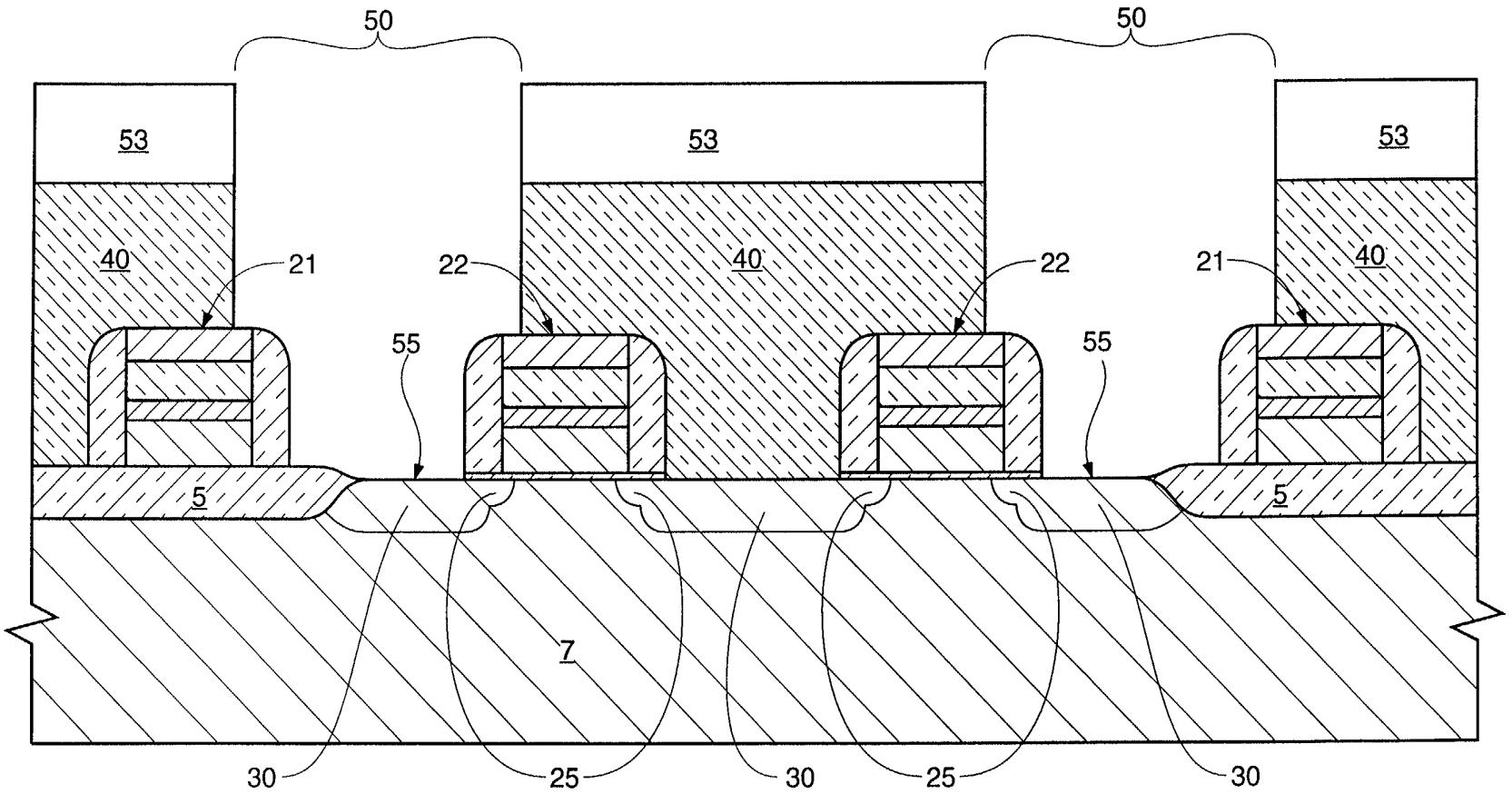

FIG. 4

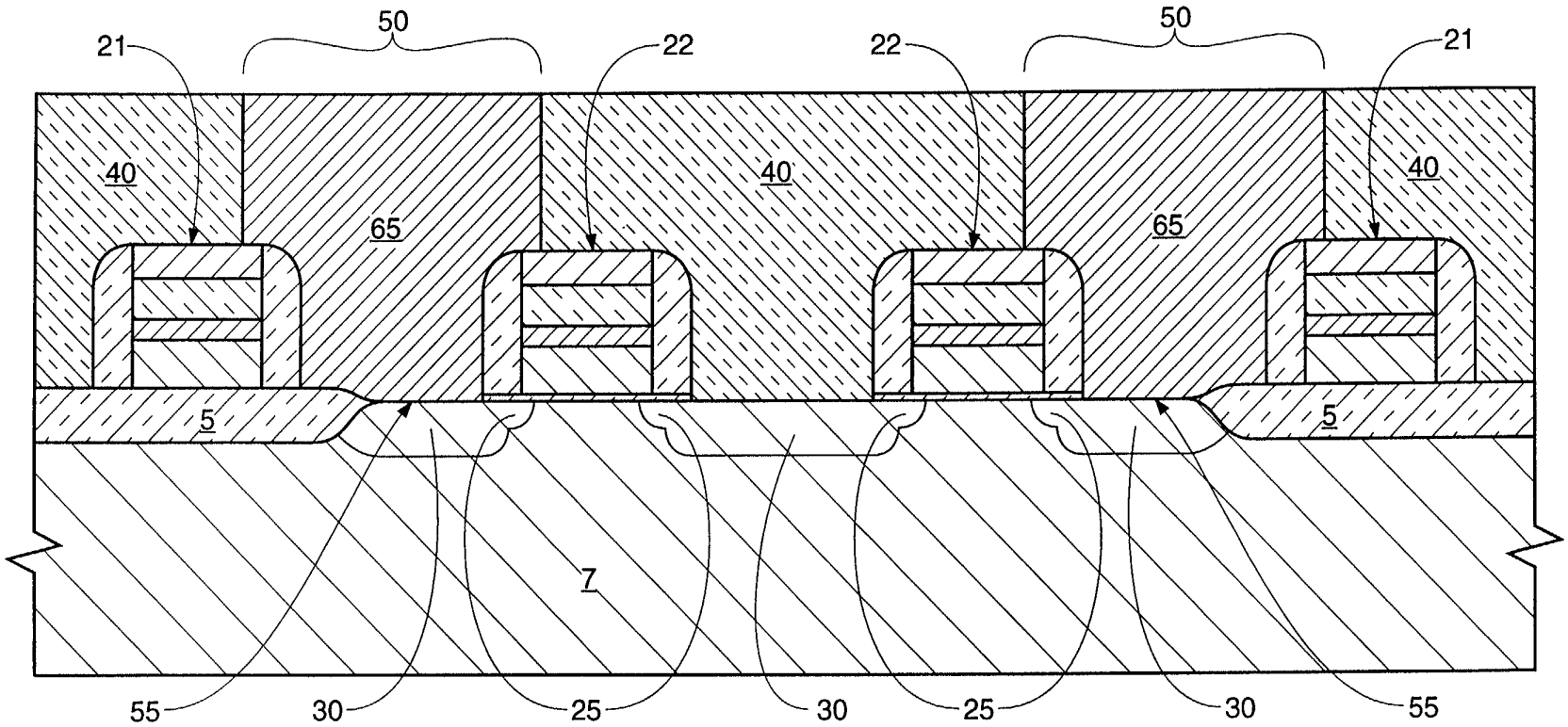

FIG. 5

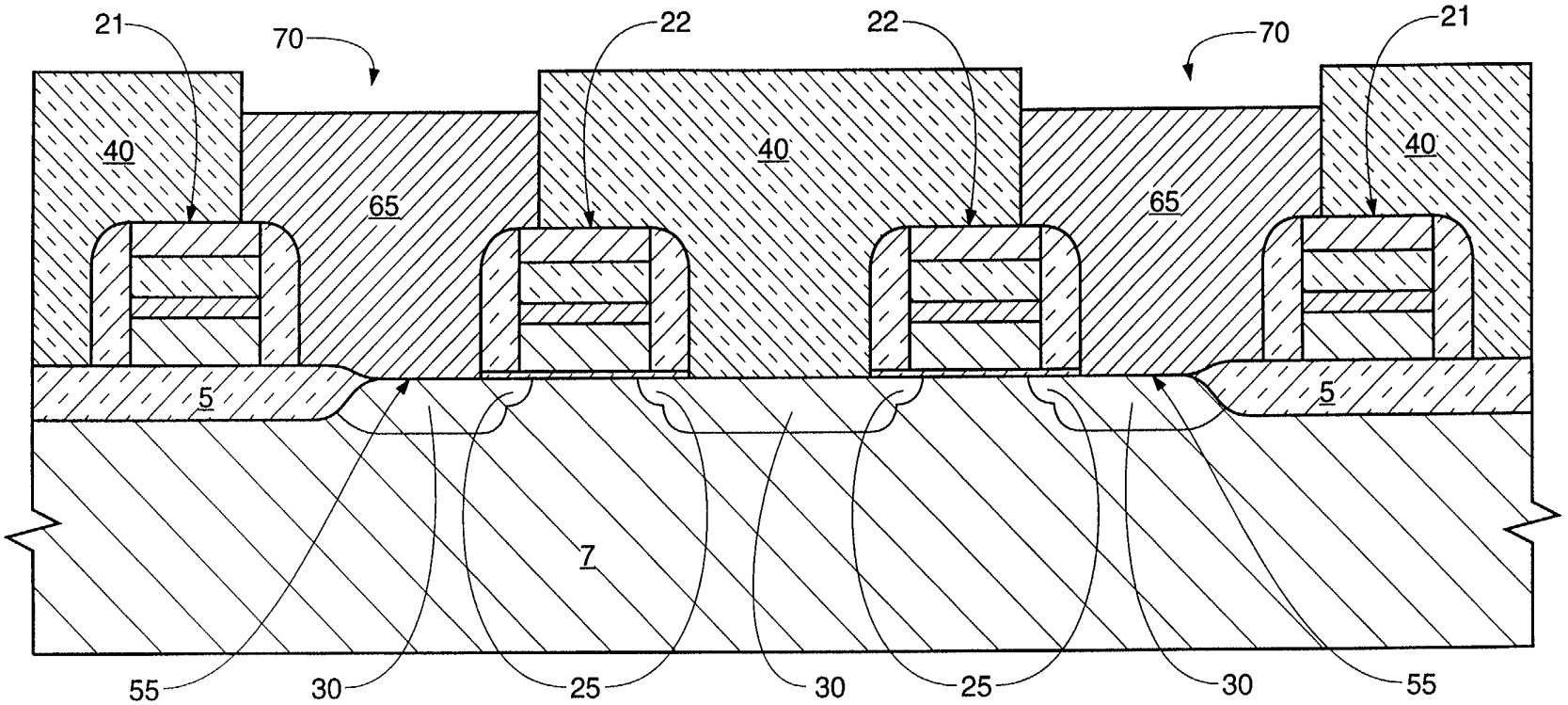

FIG. 6

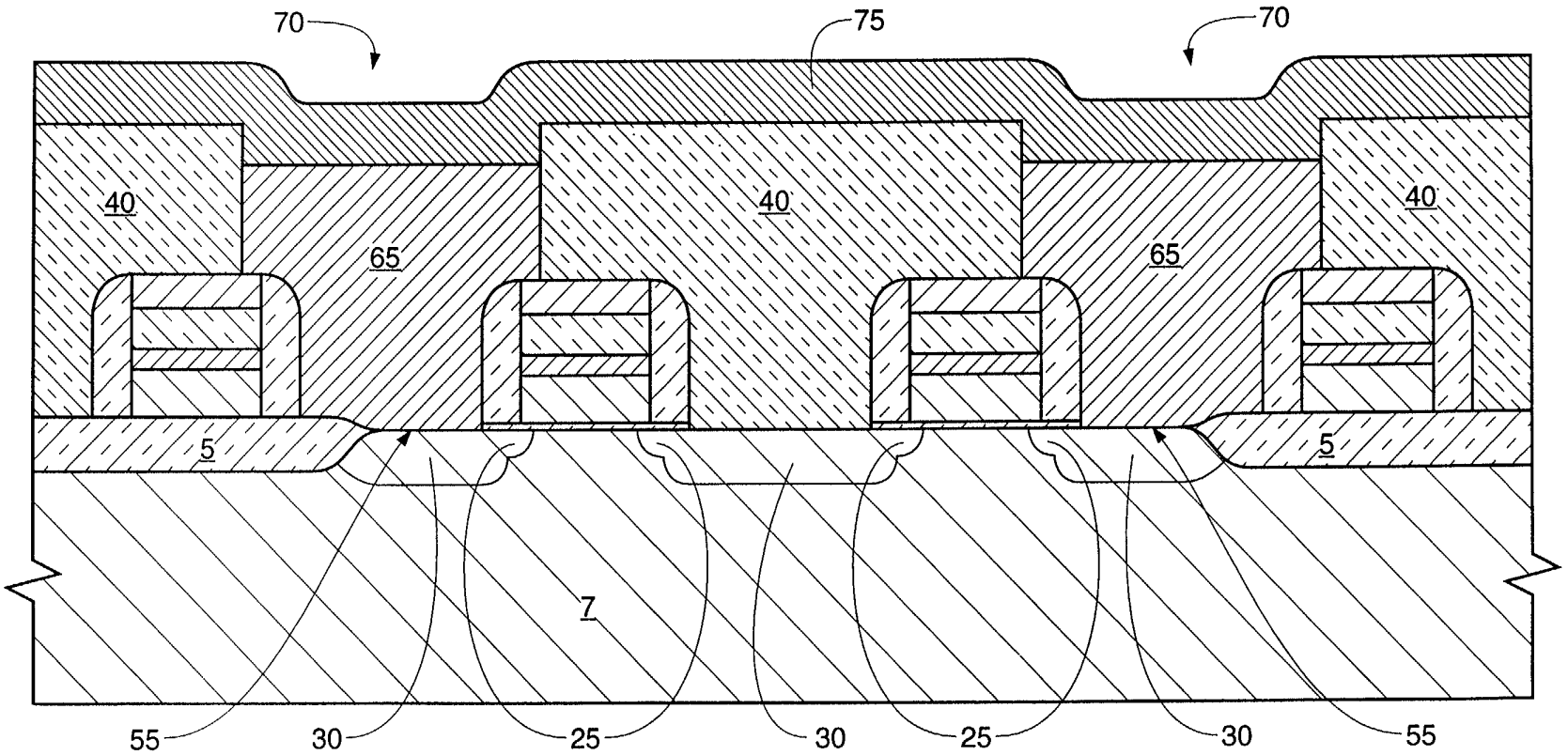

FIG. 7A

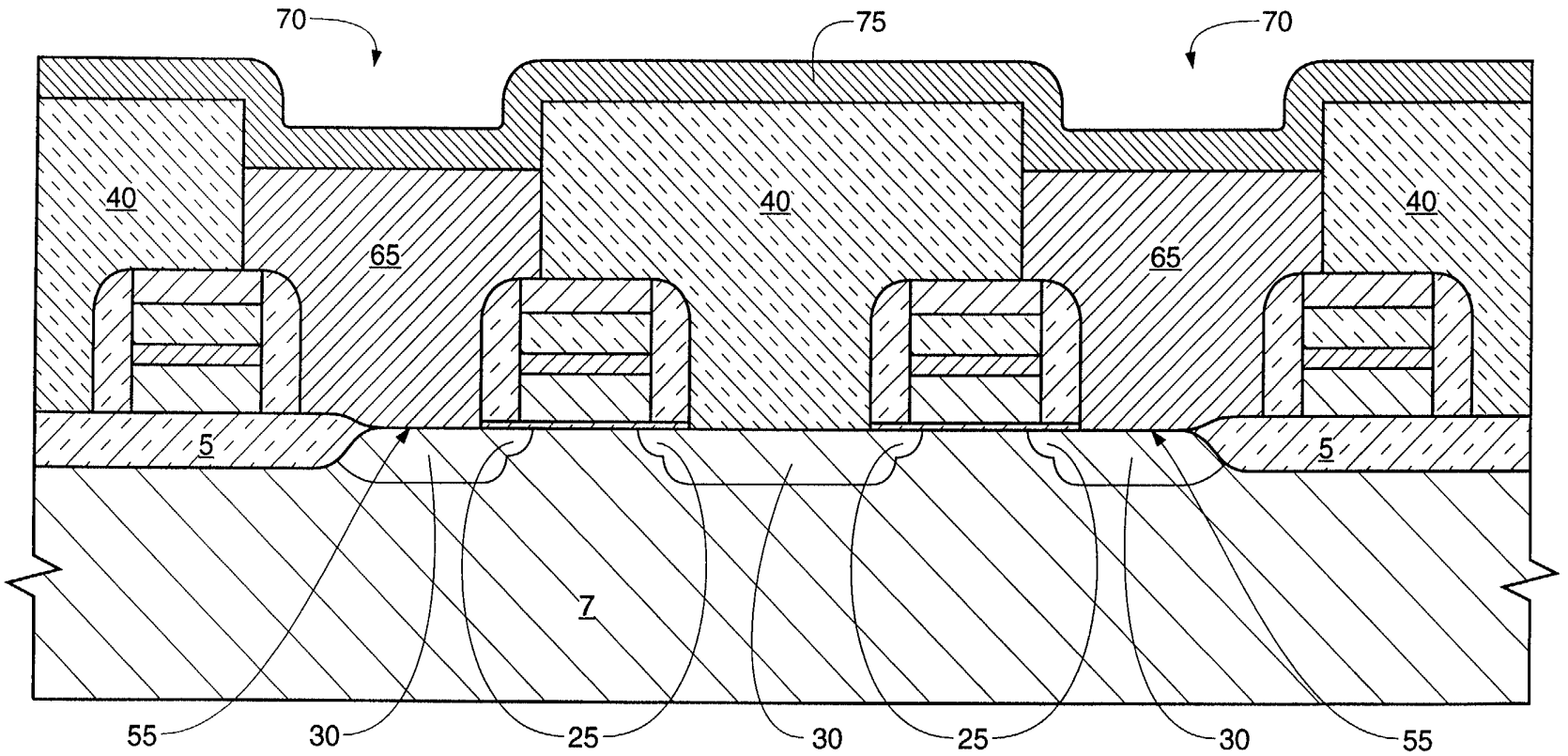

FIG. 7B

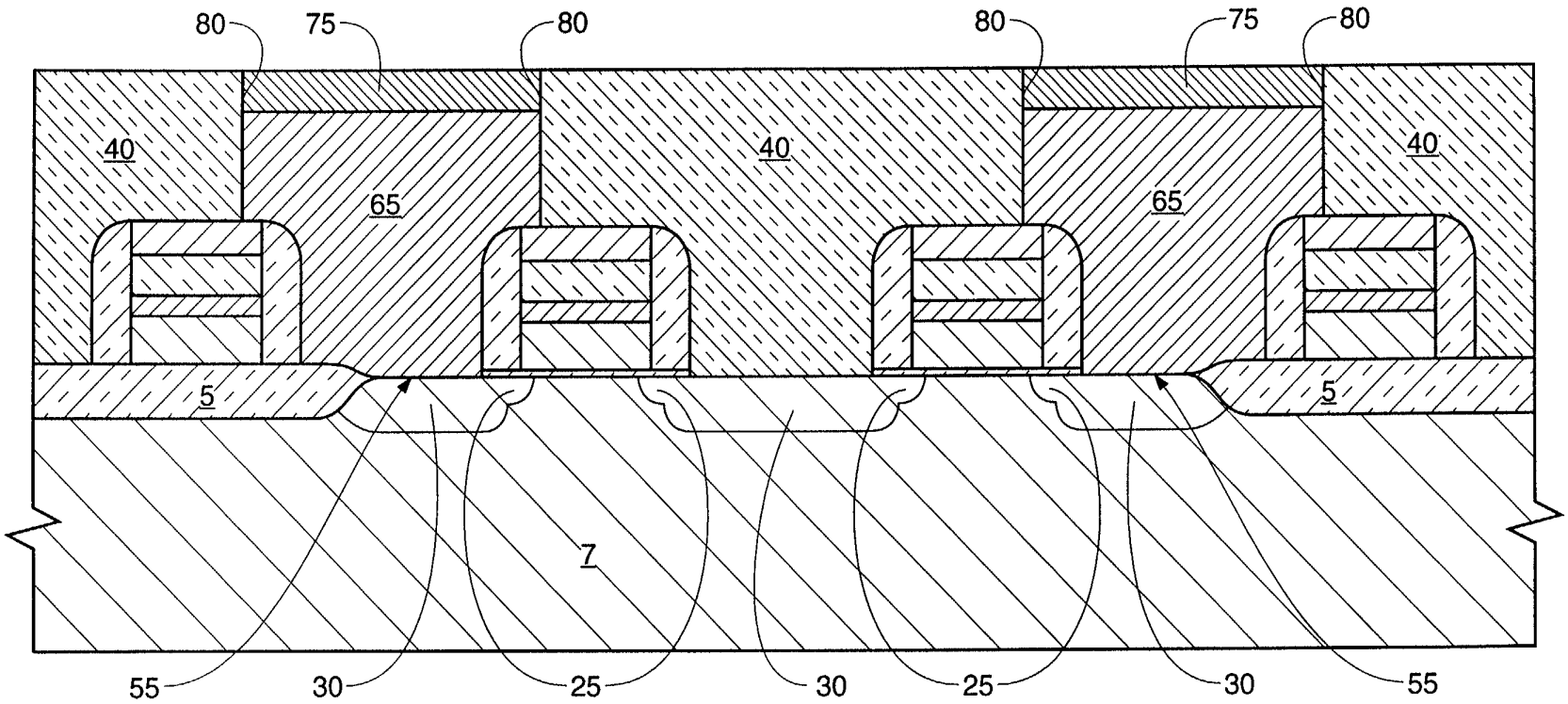

FIG. 8A

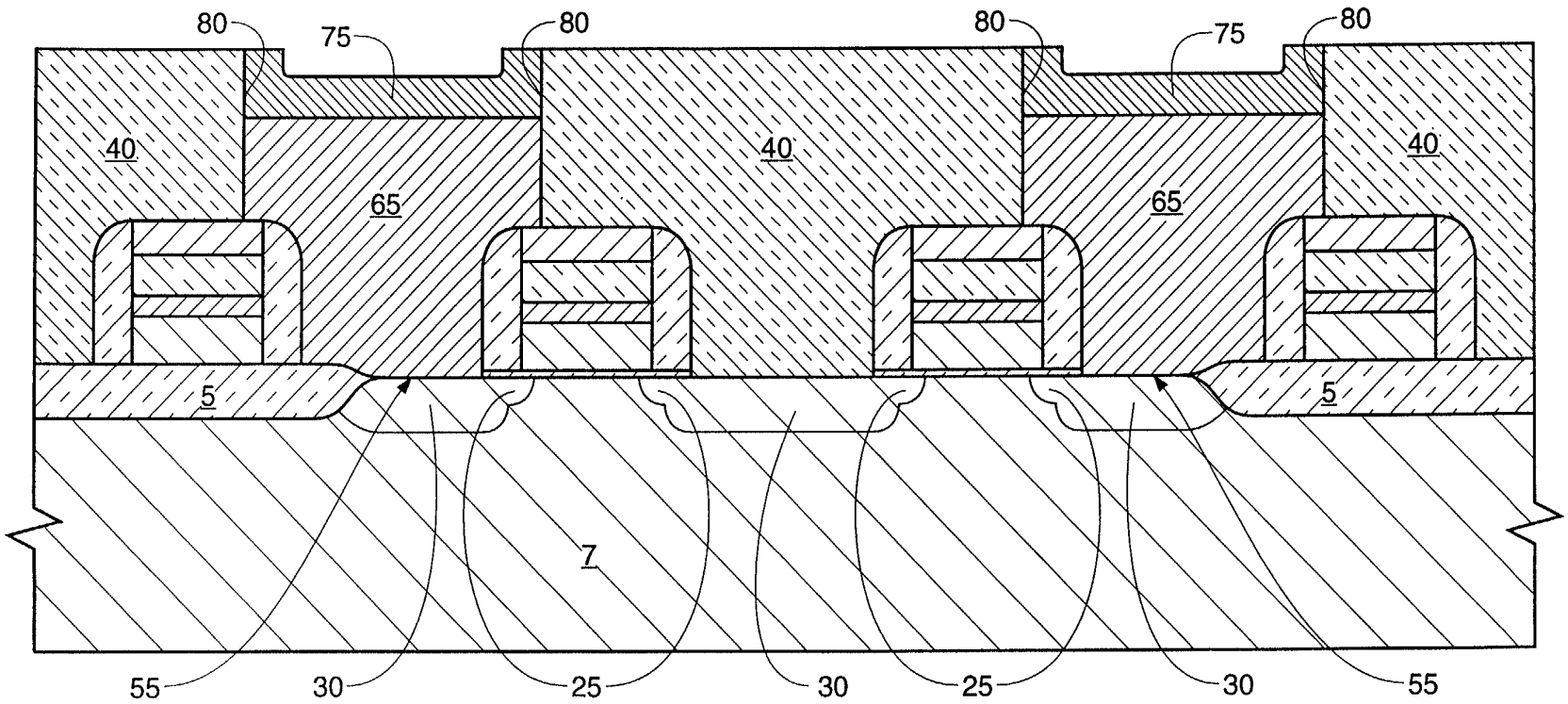

FIG. 8B

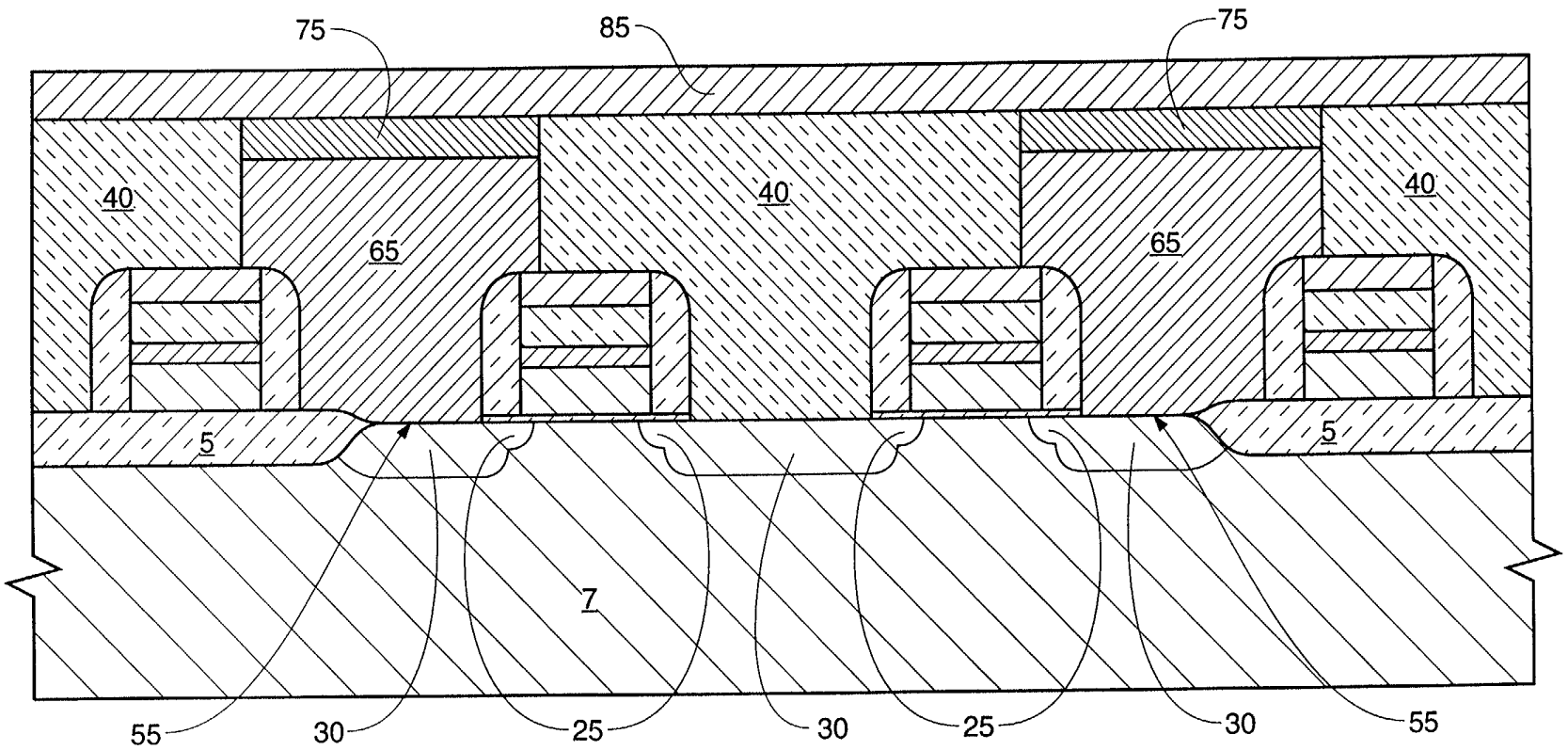

FIG. 9A

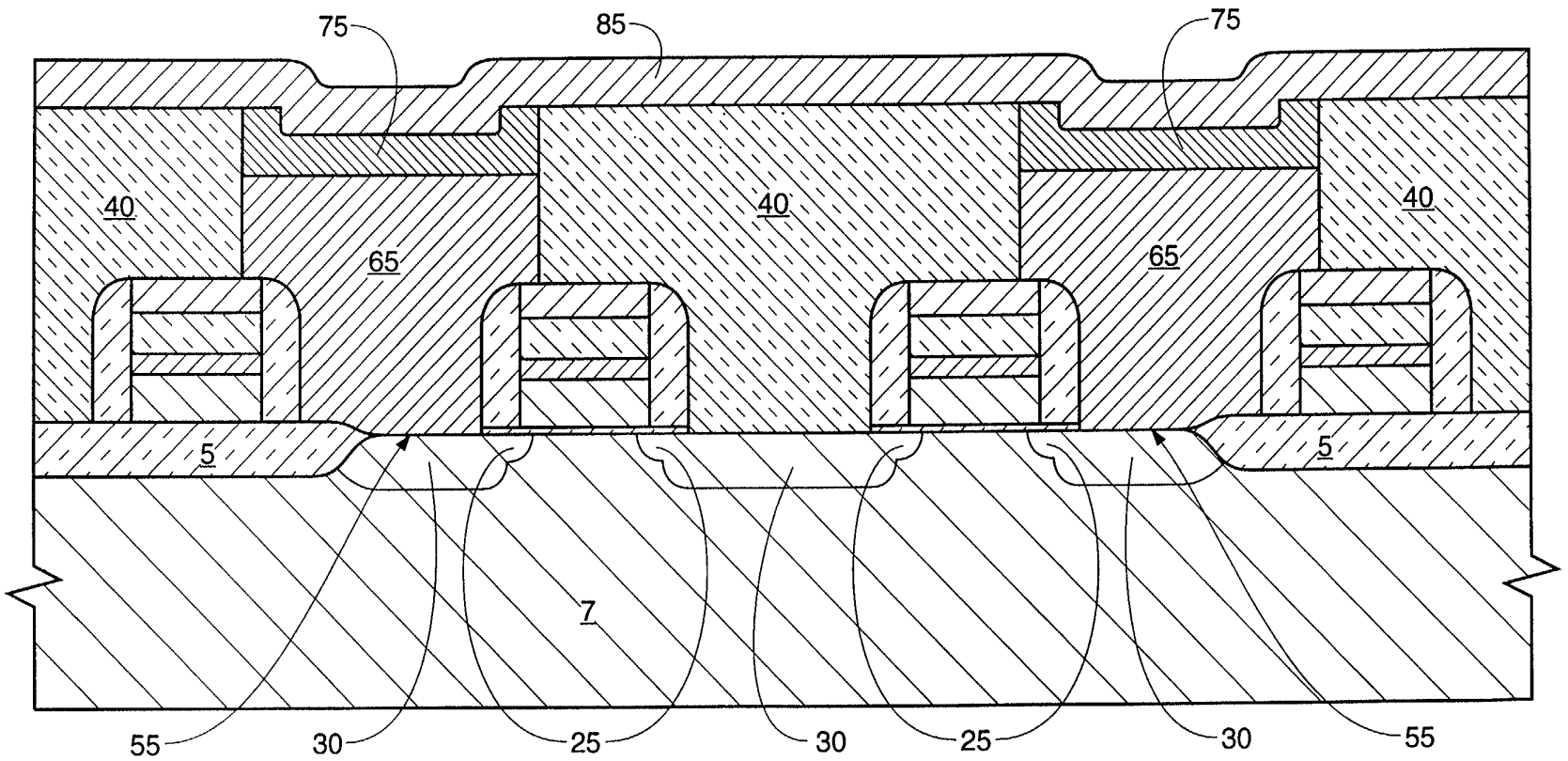

FIG. 9B

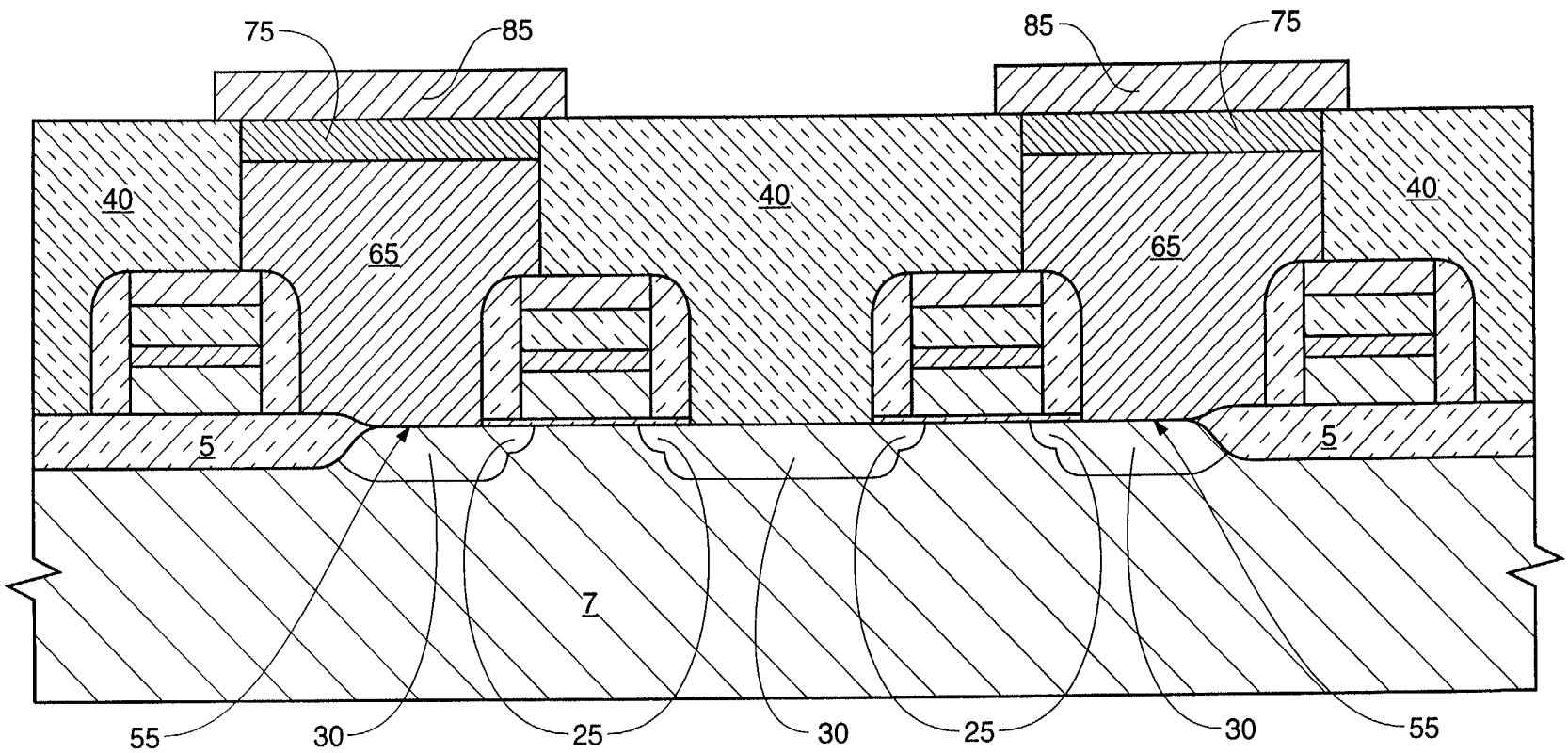

FIG. 10A

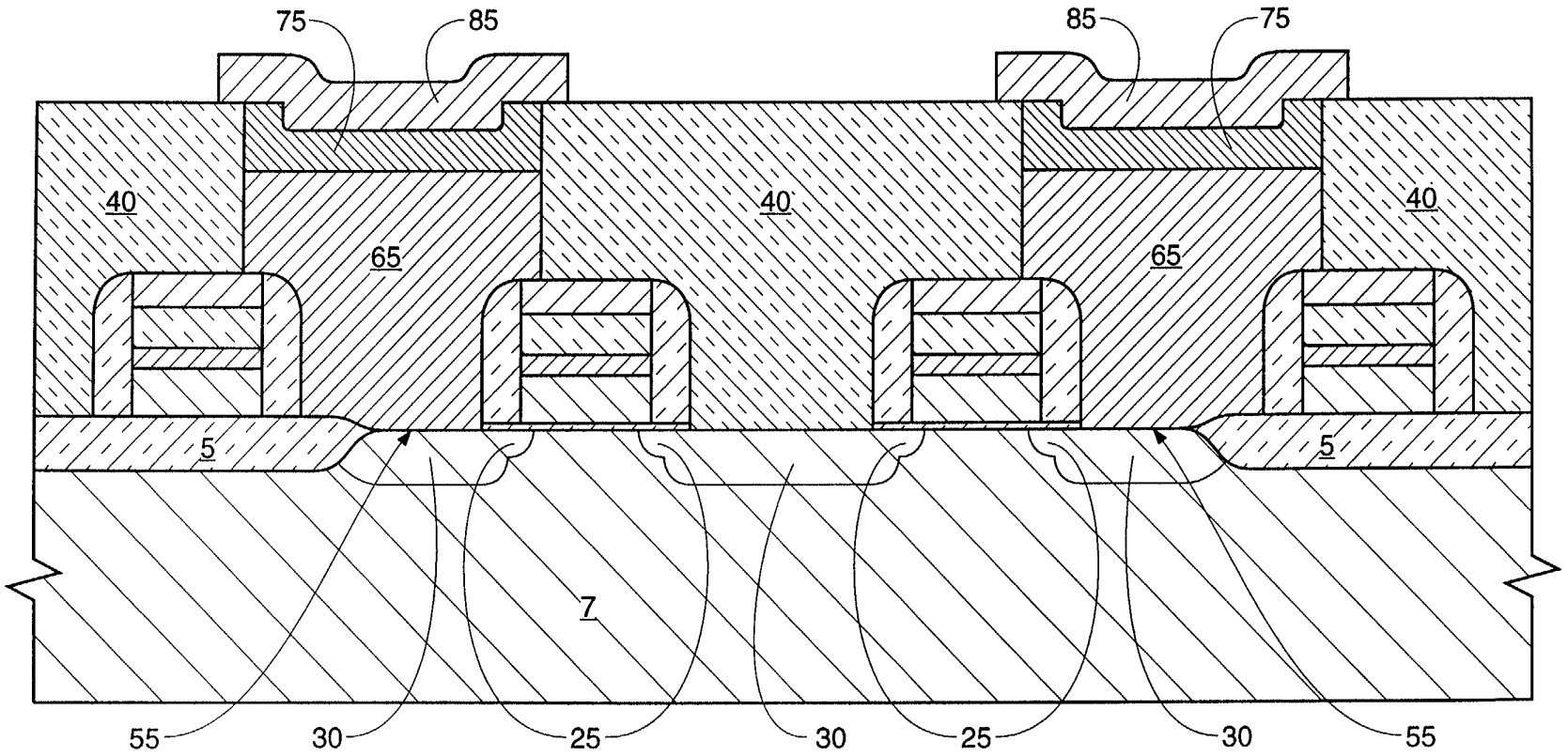

FIG. 10B

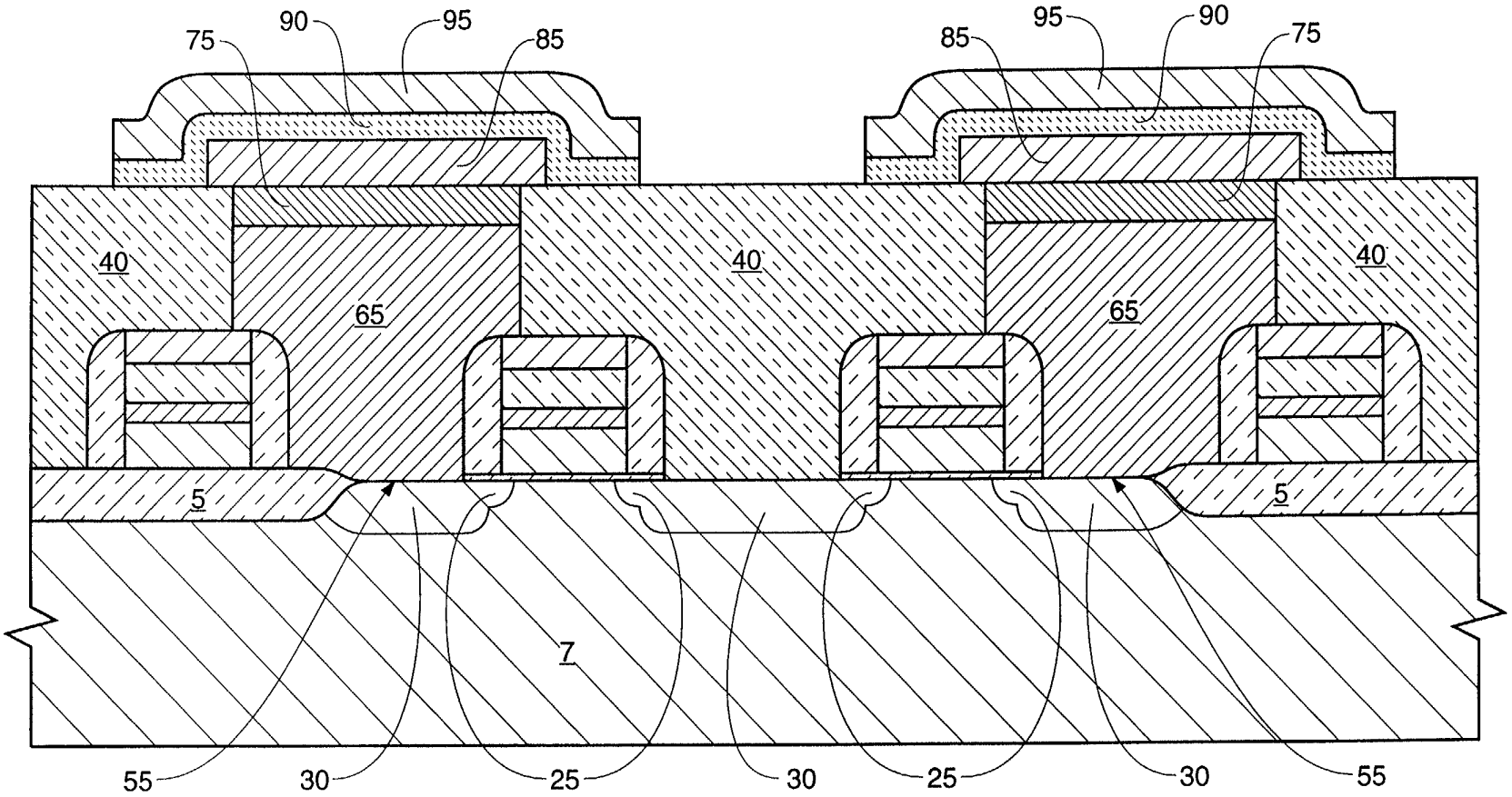

FIG. 11A

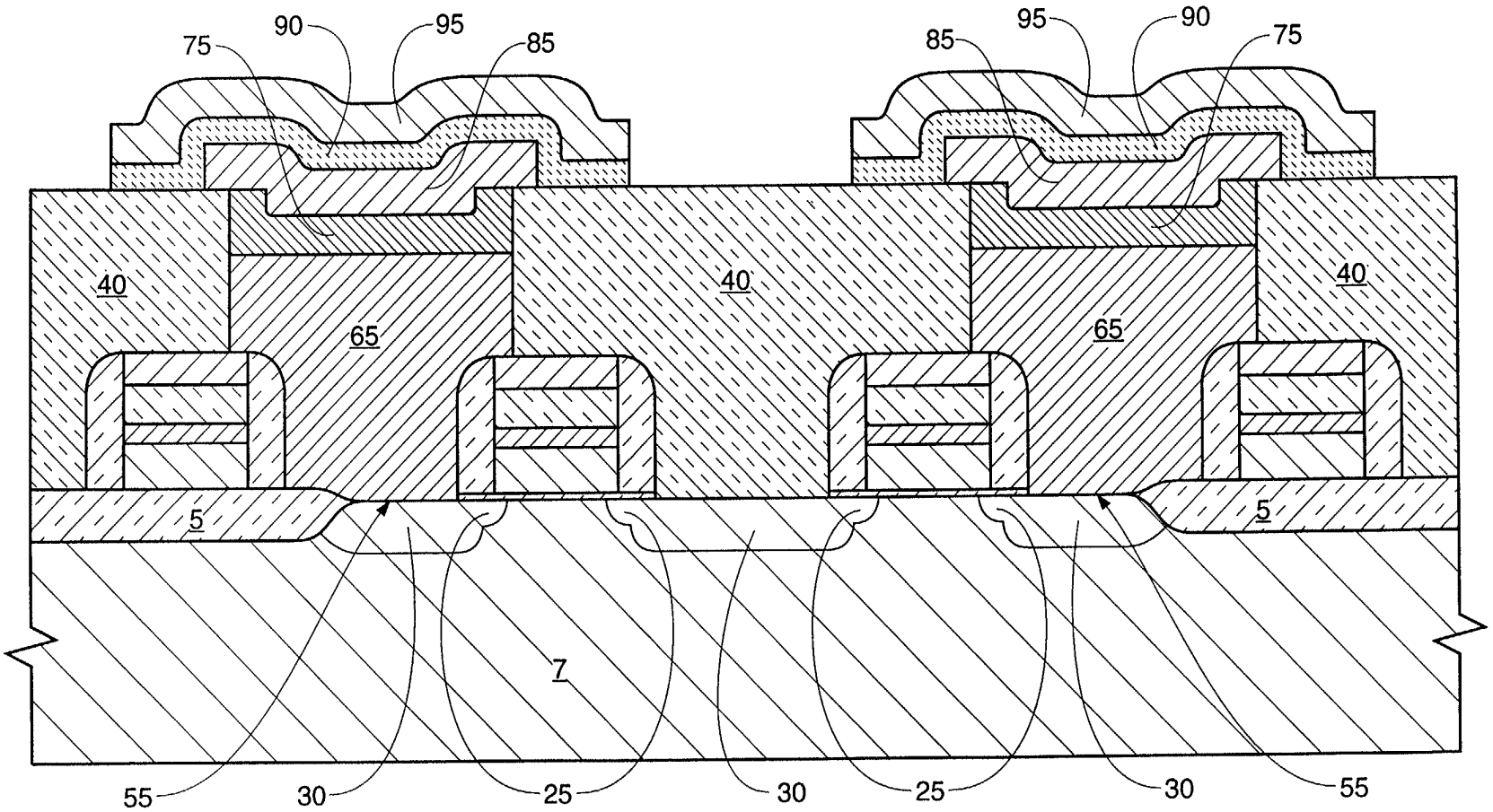

FIG. 11B

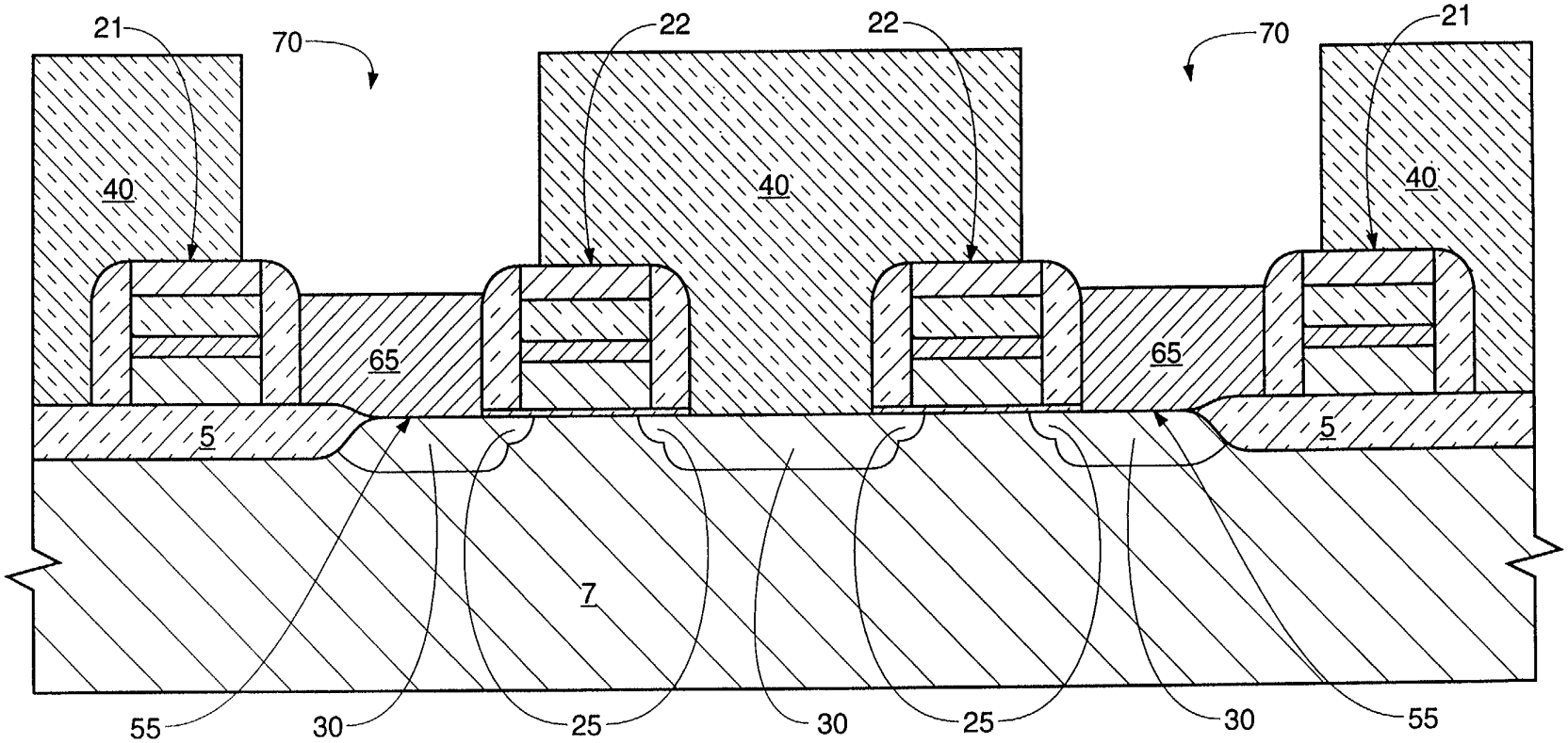

FIG. 12

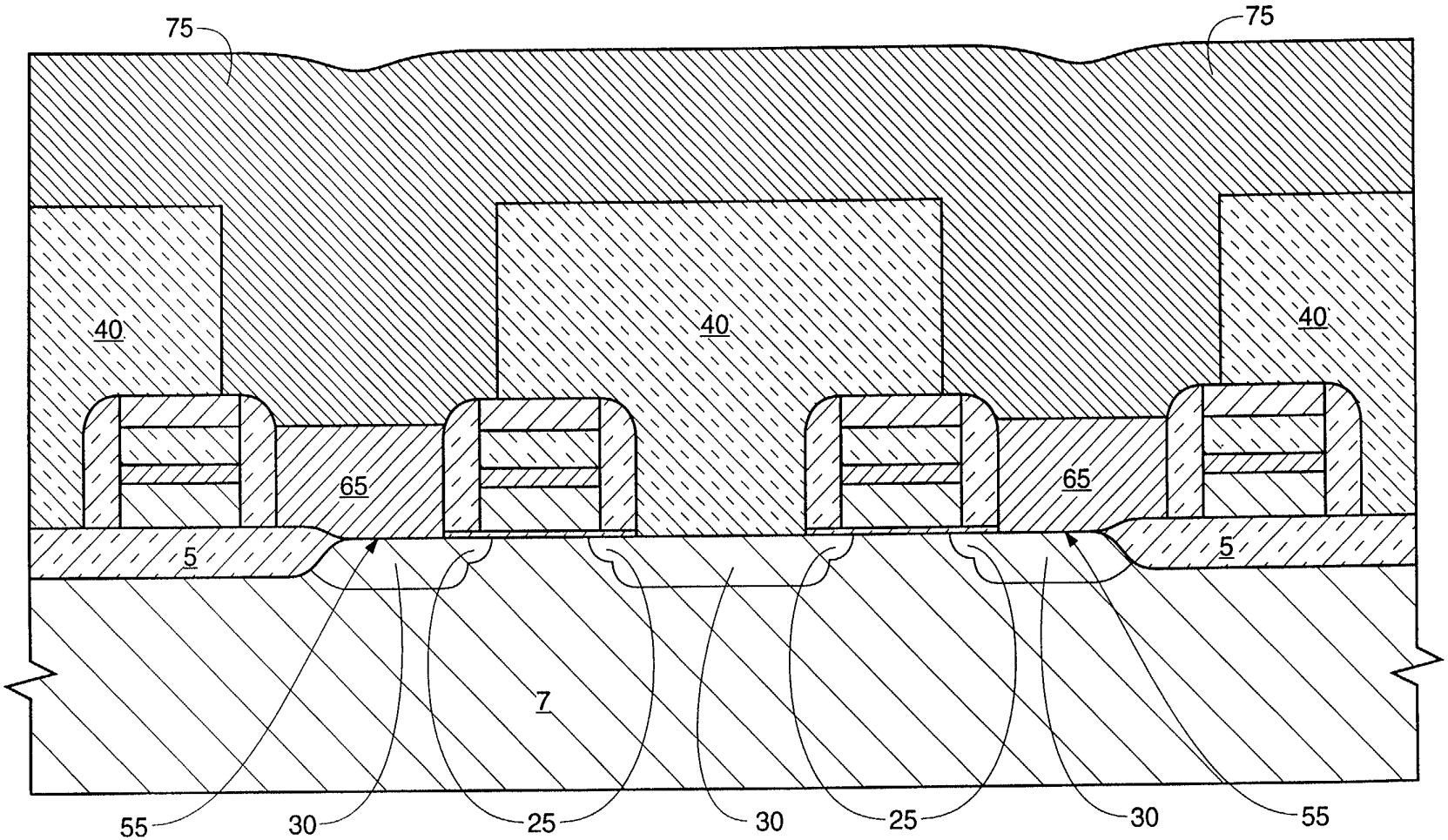

FIG. 13

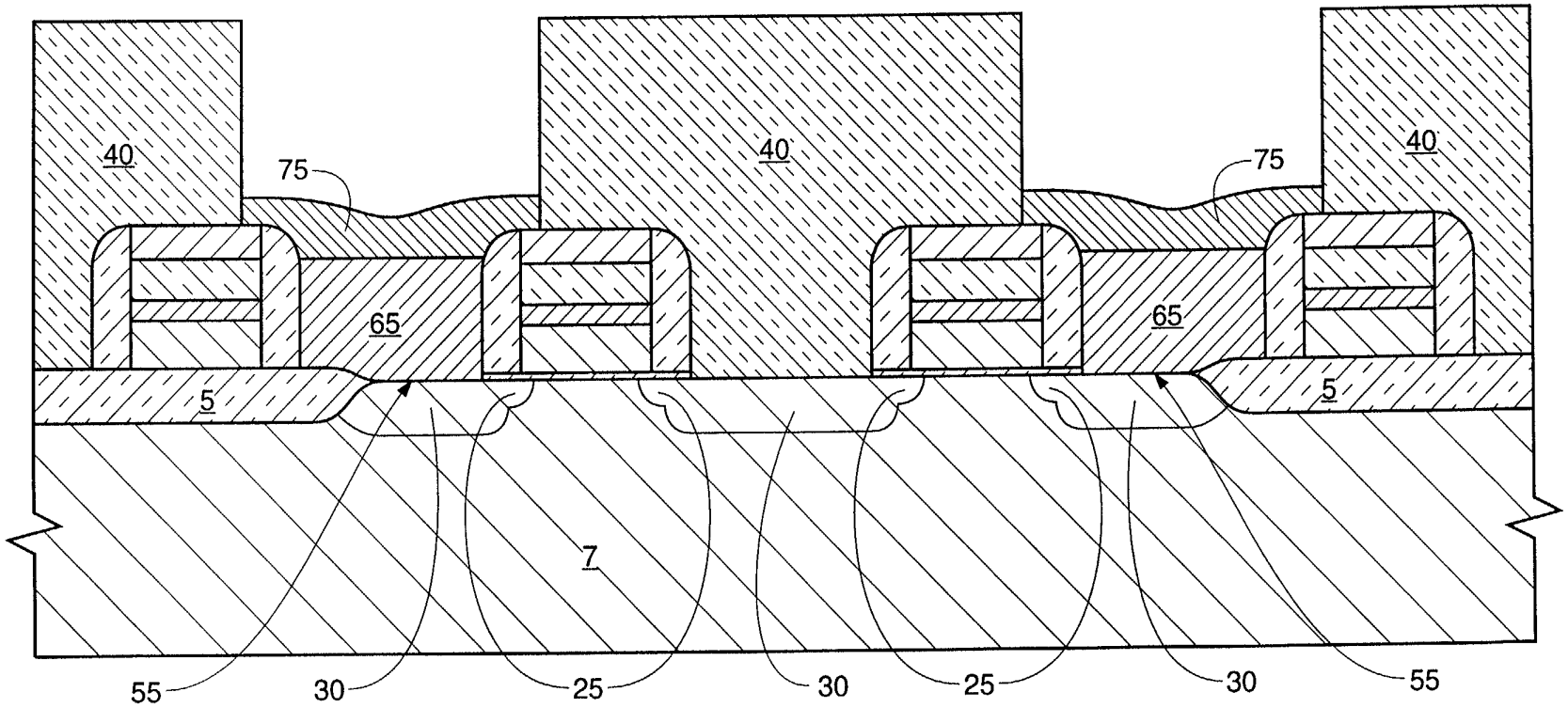

FIG. 14

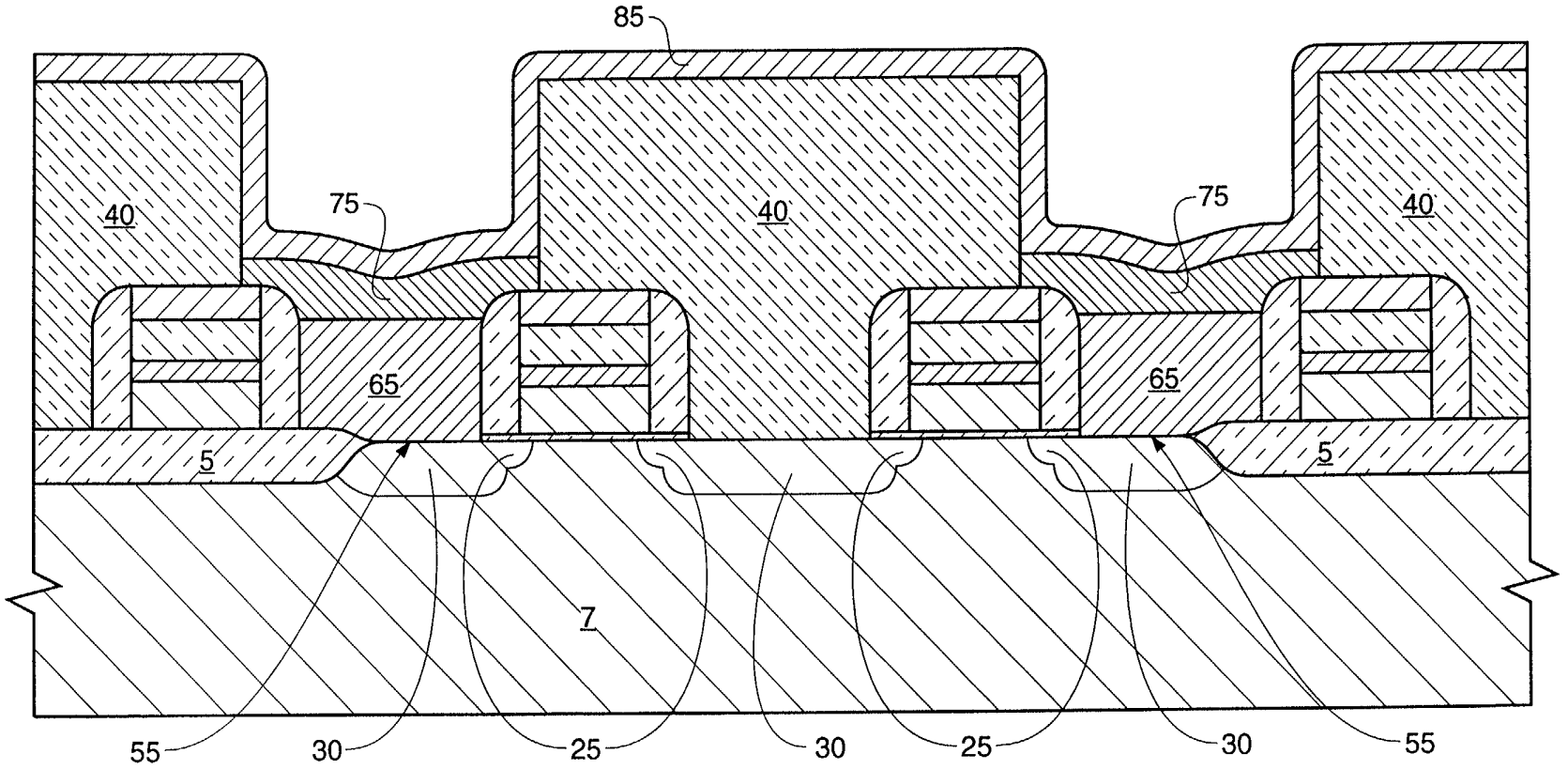

FIG. 15

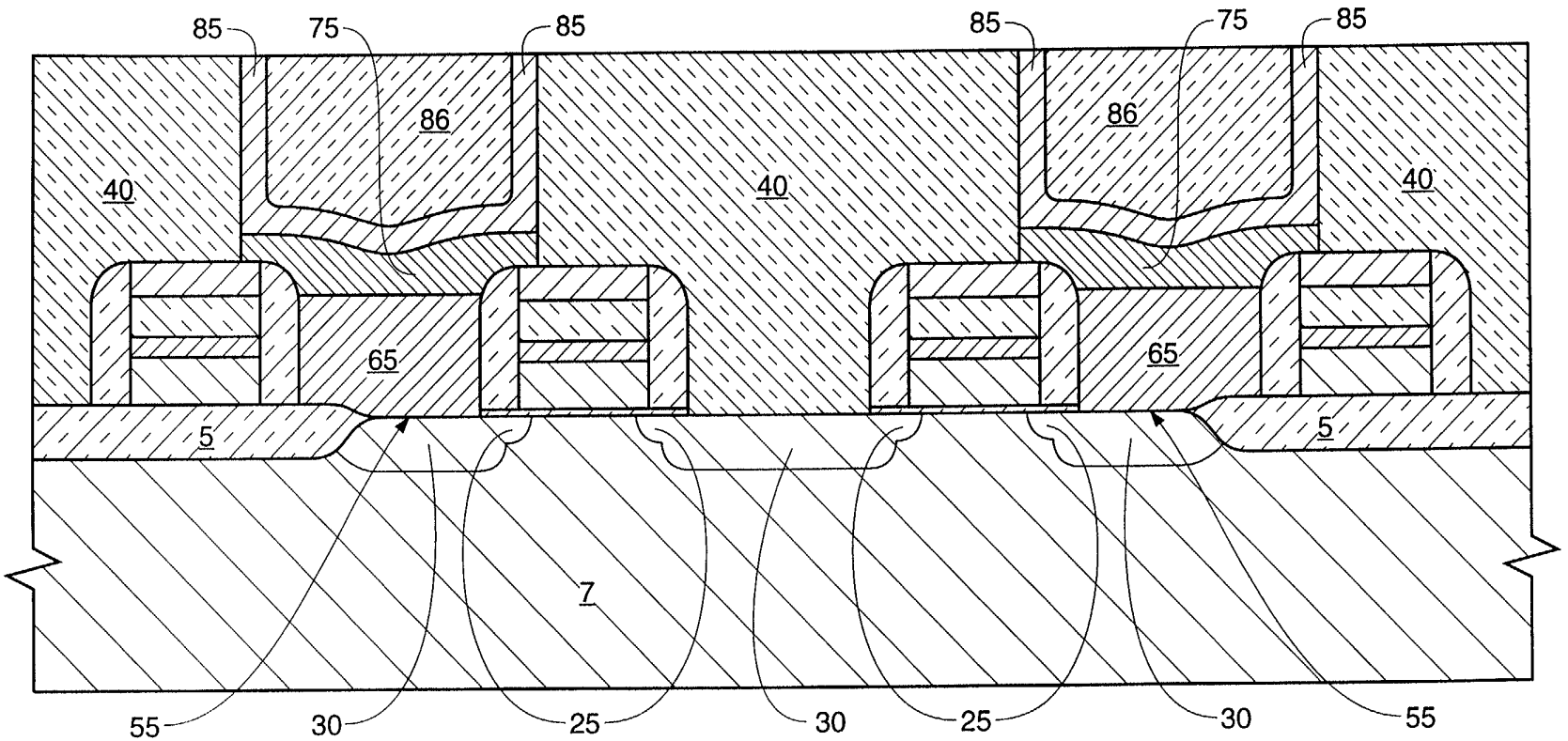

FIG. 16

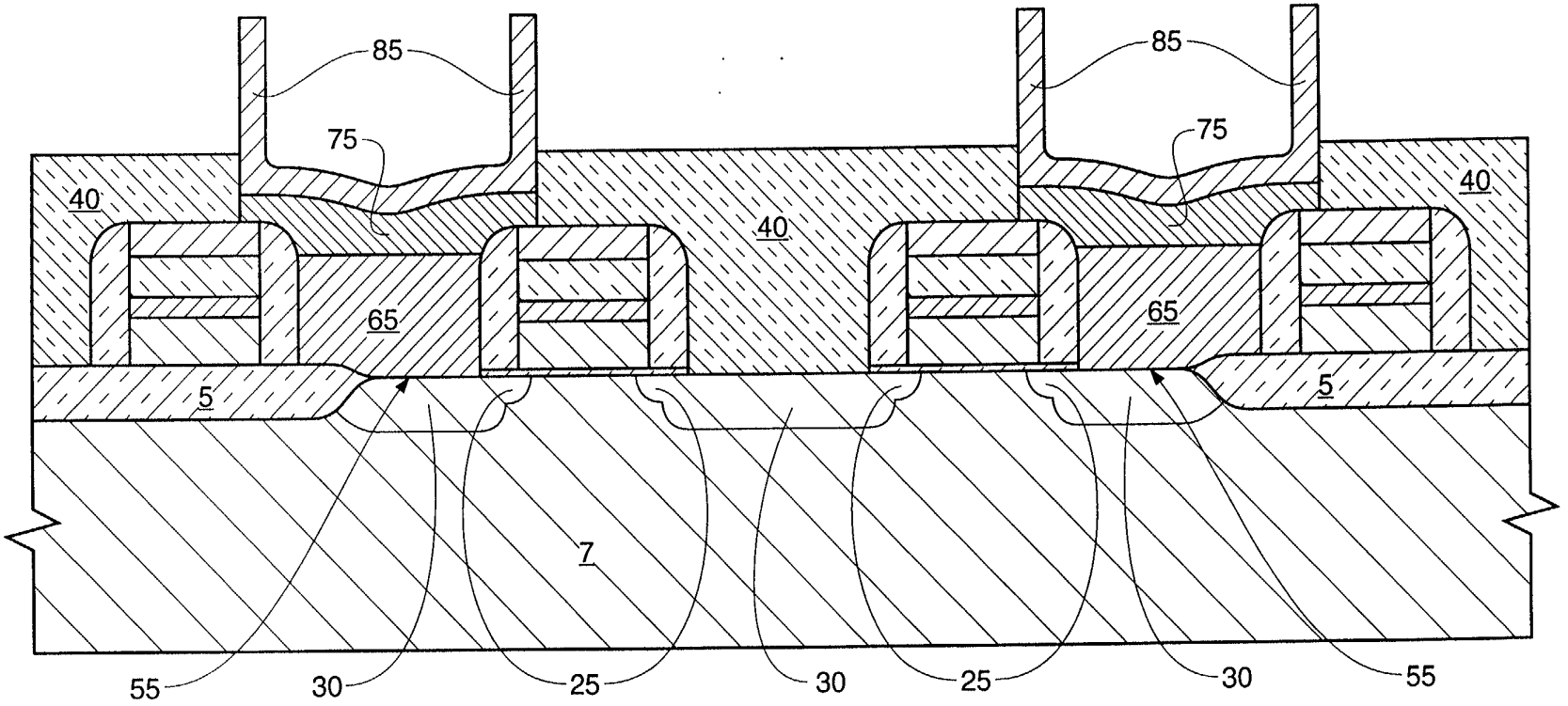

FIG. 17

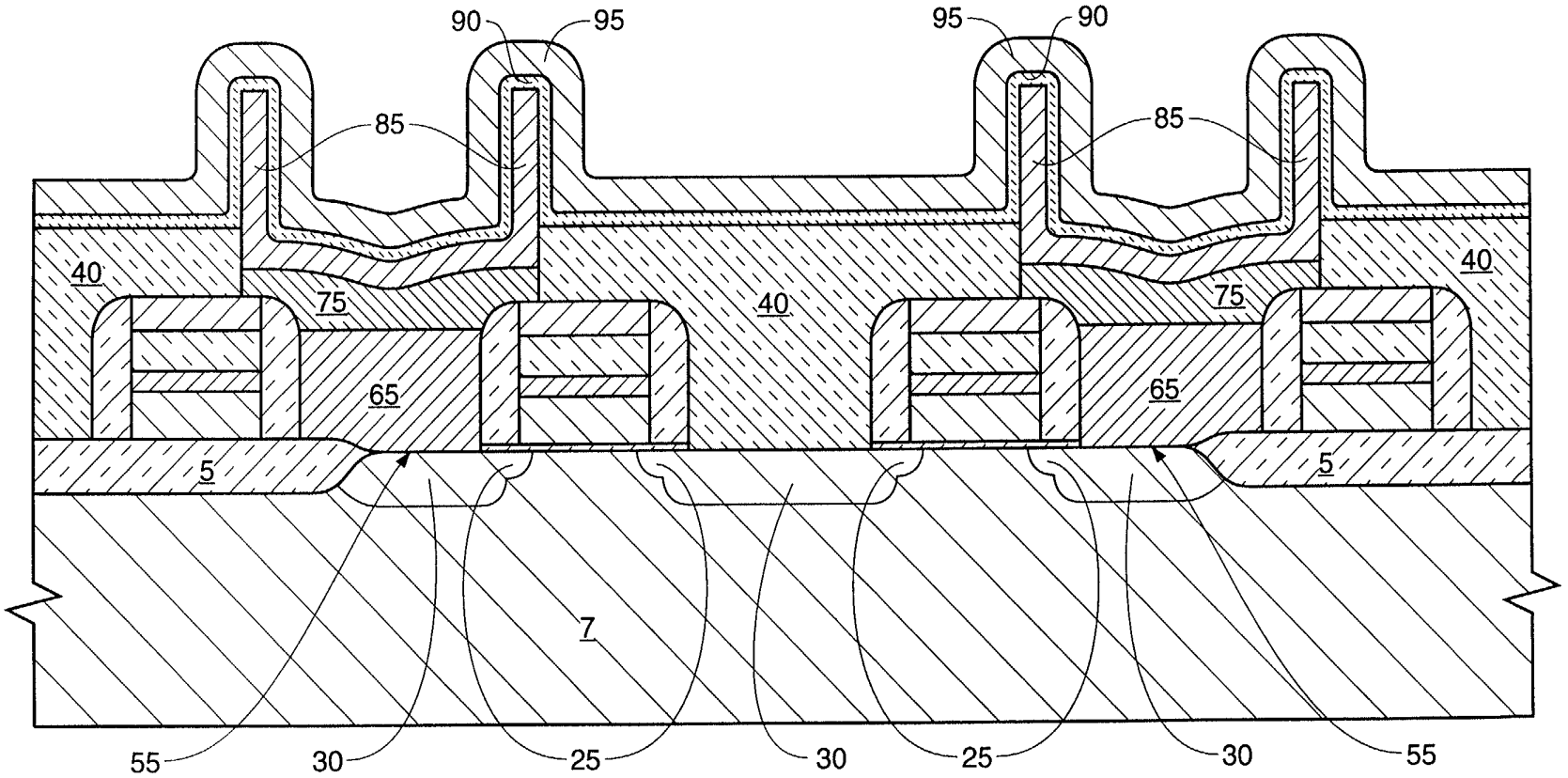

FIG. 18

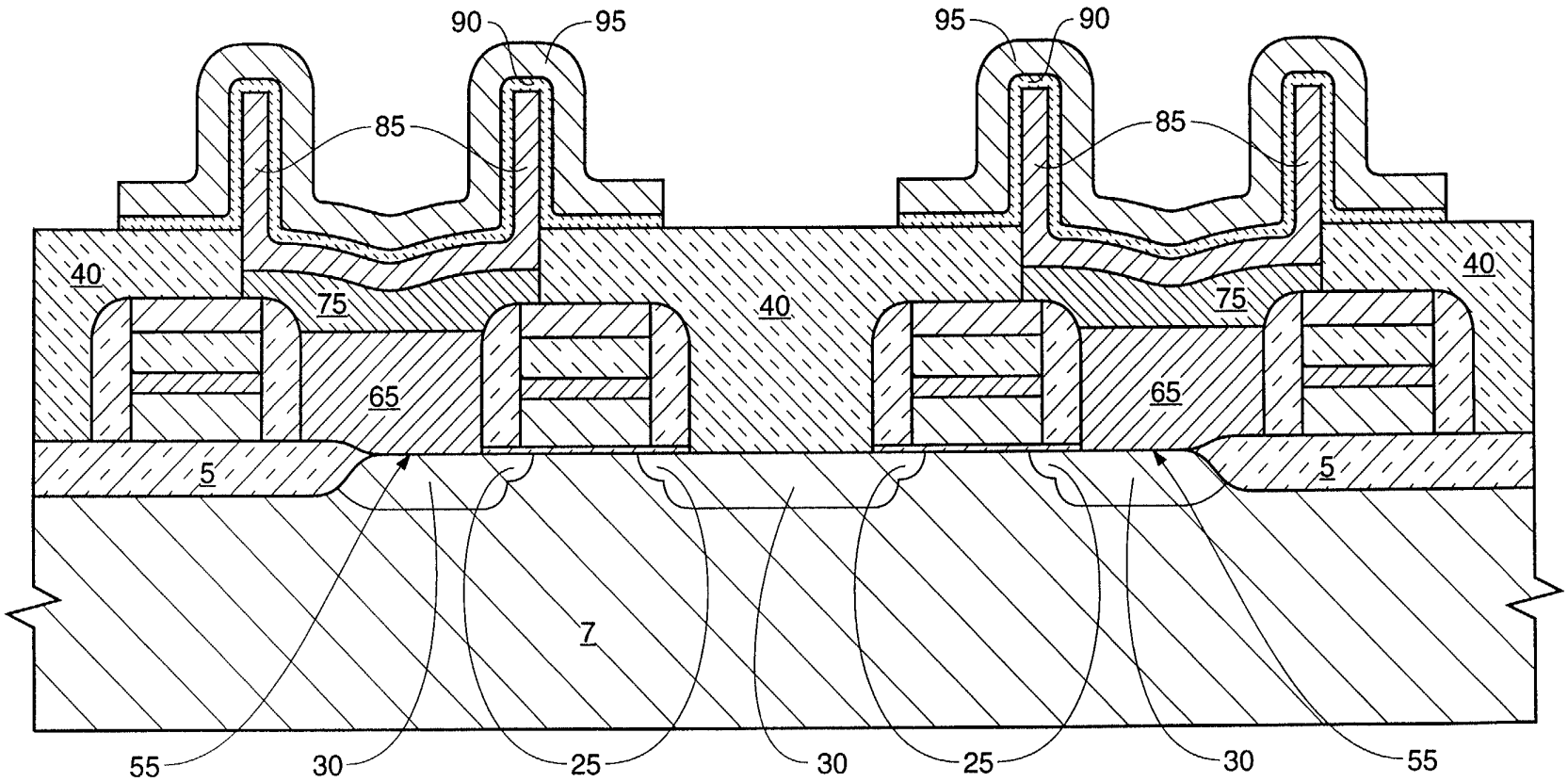

FIG. 19

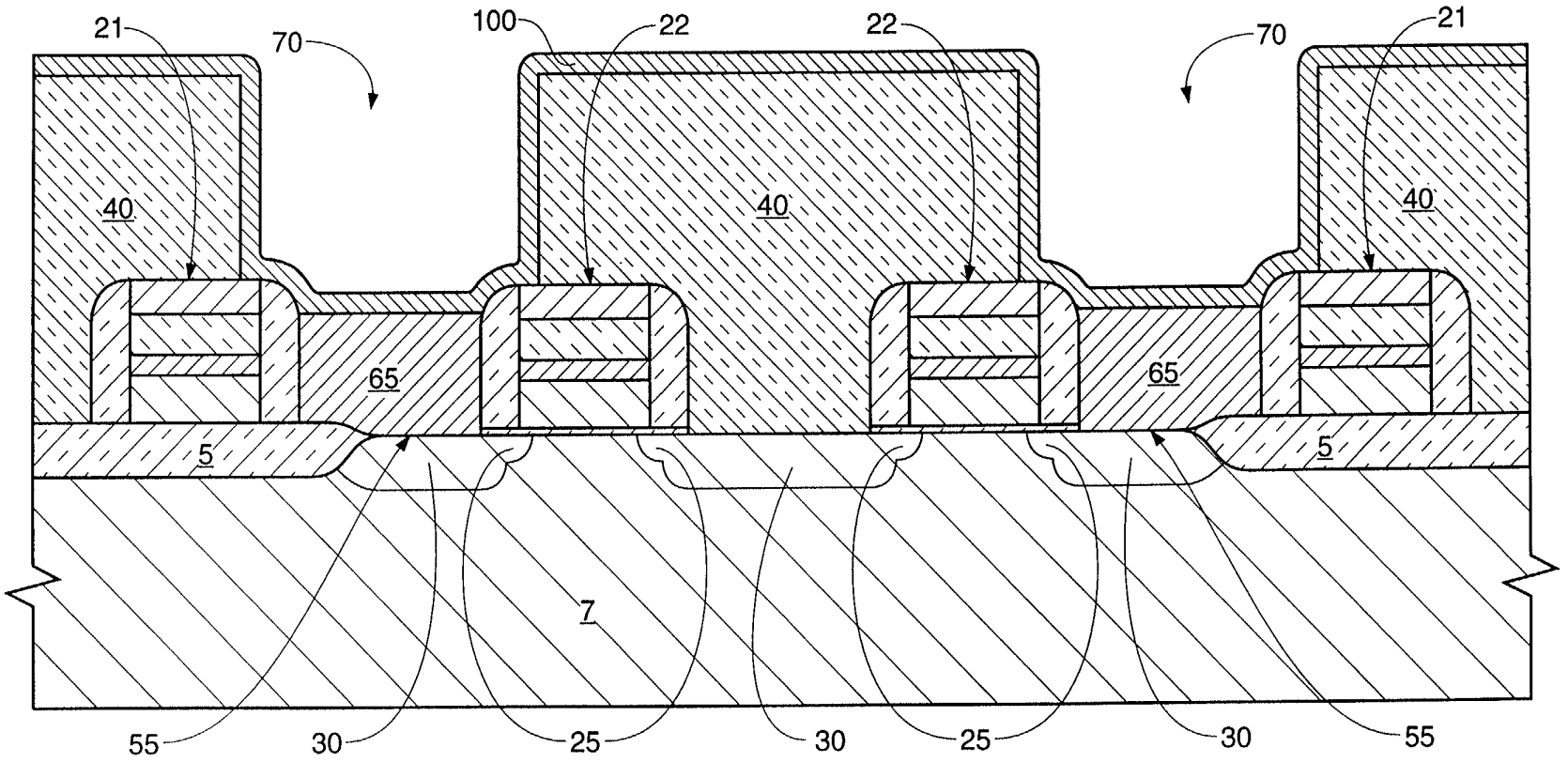

FIG. 20

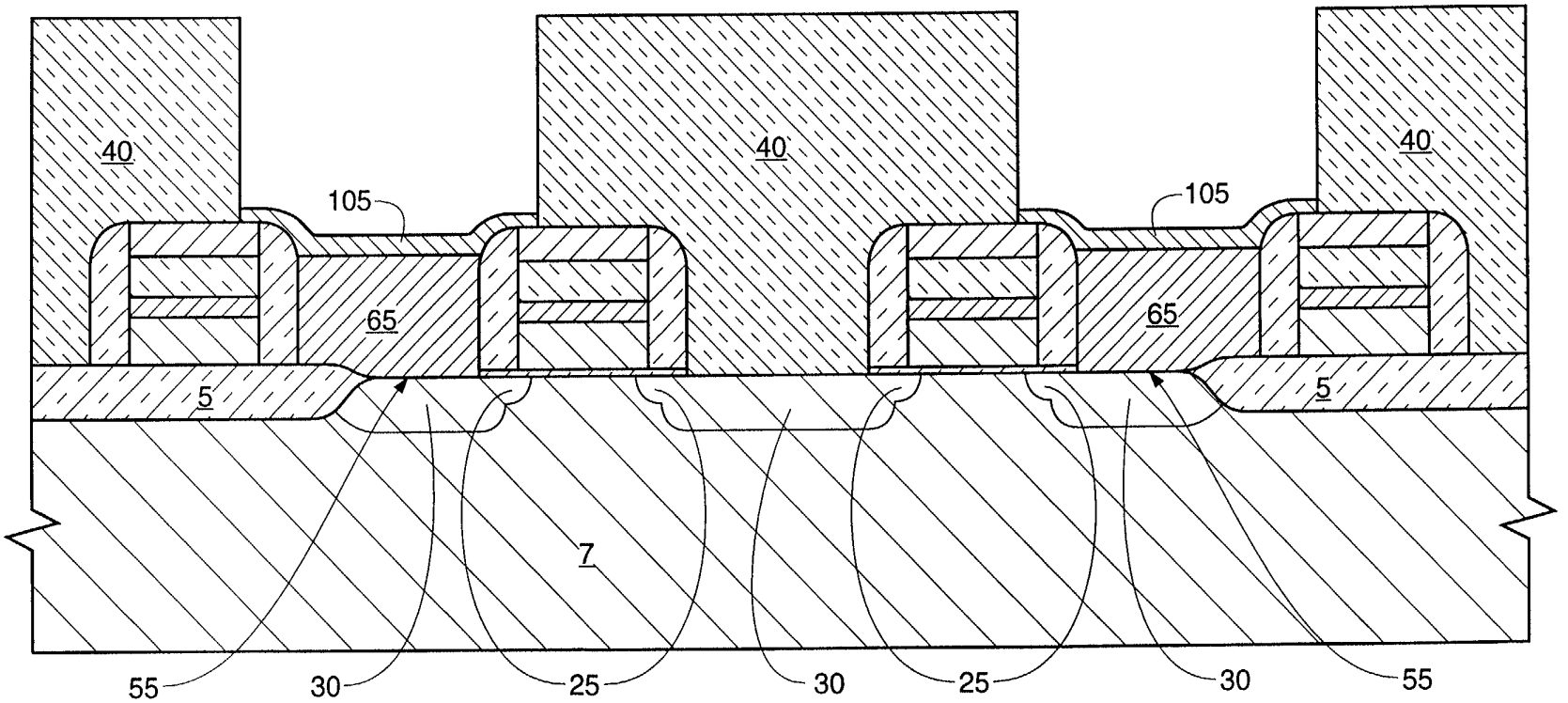

FIG. 21

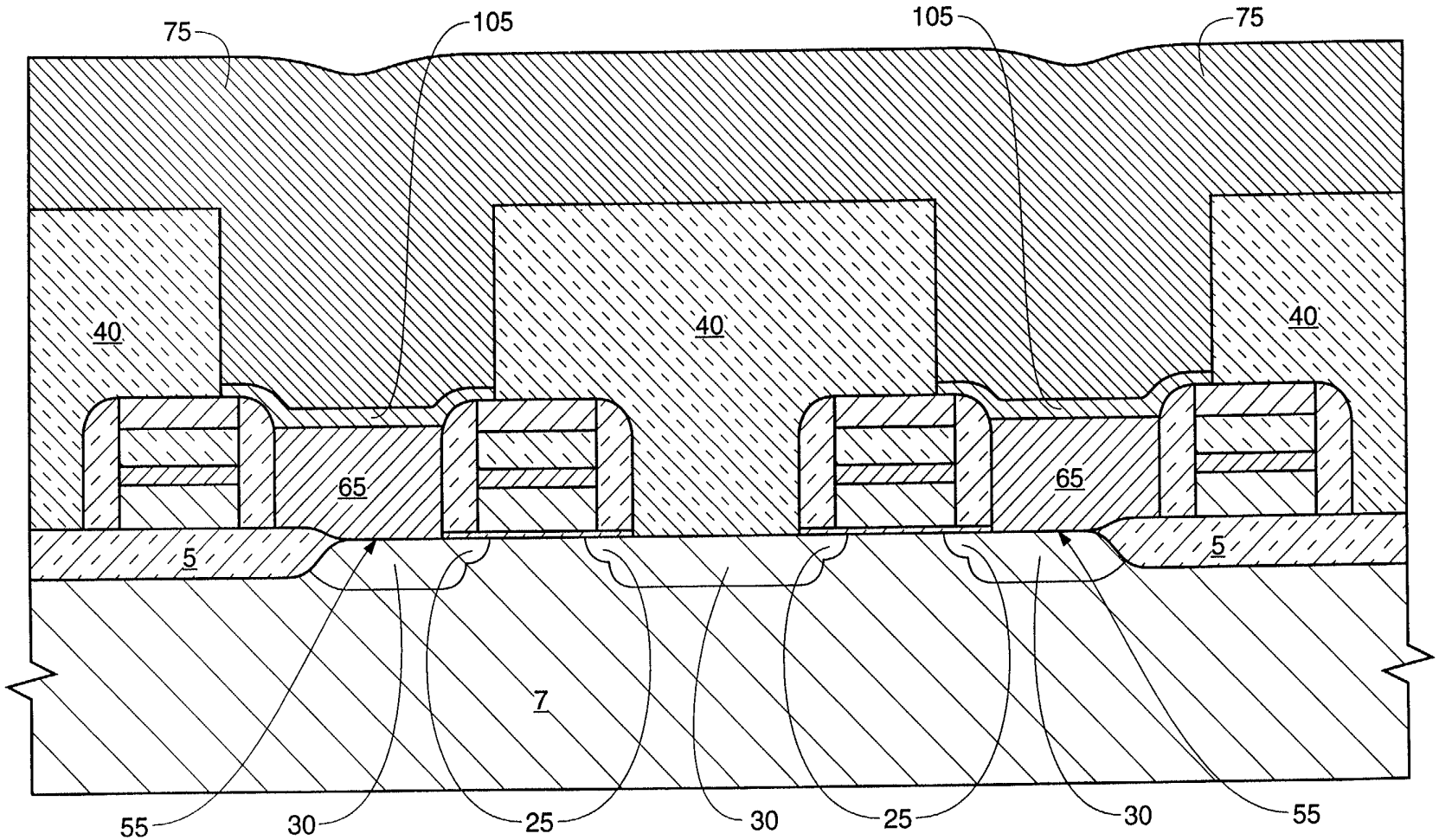

FIG. 22

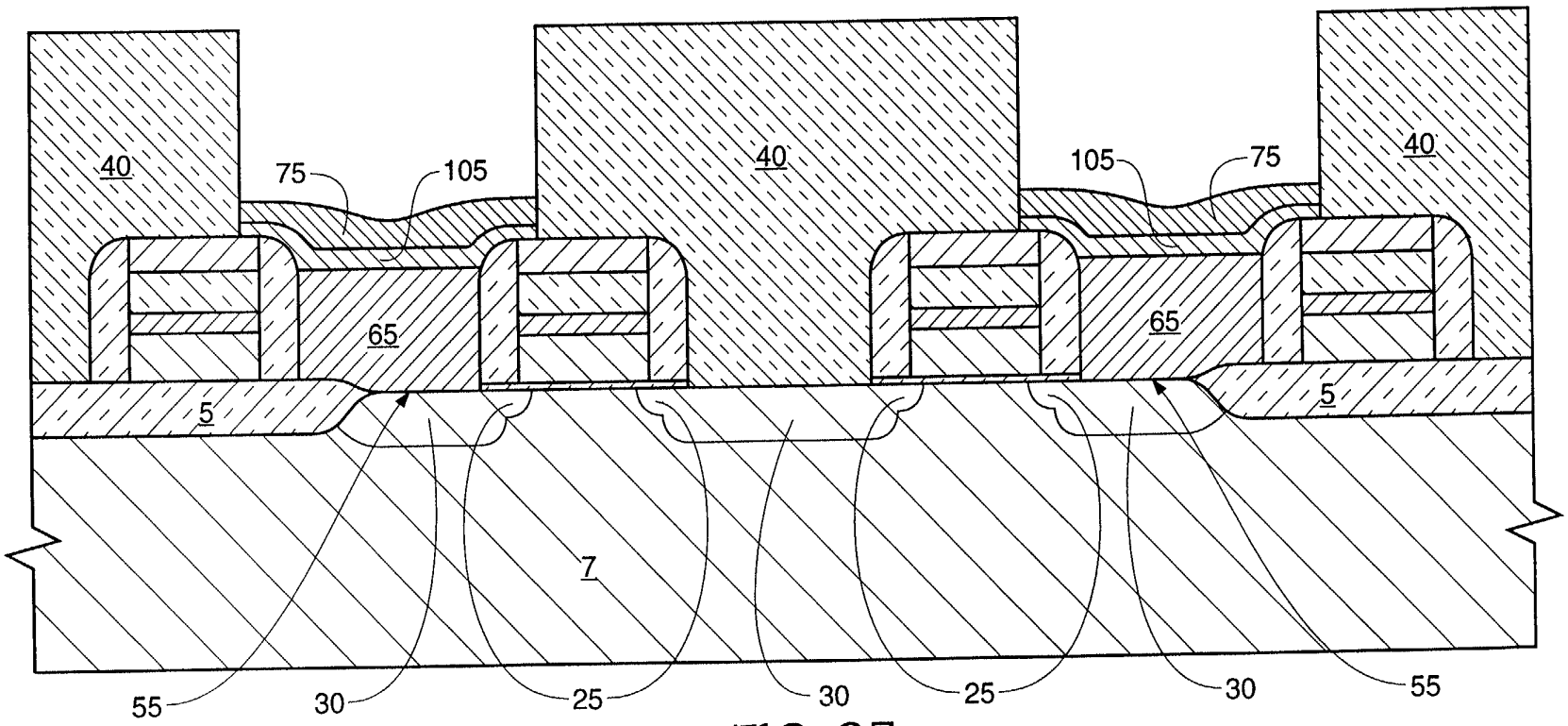

FIG. 23

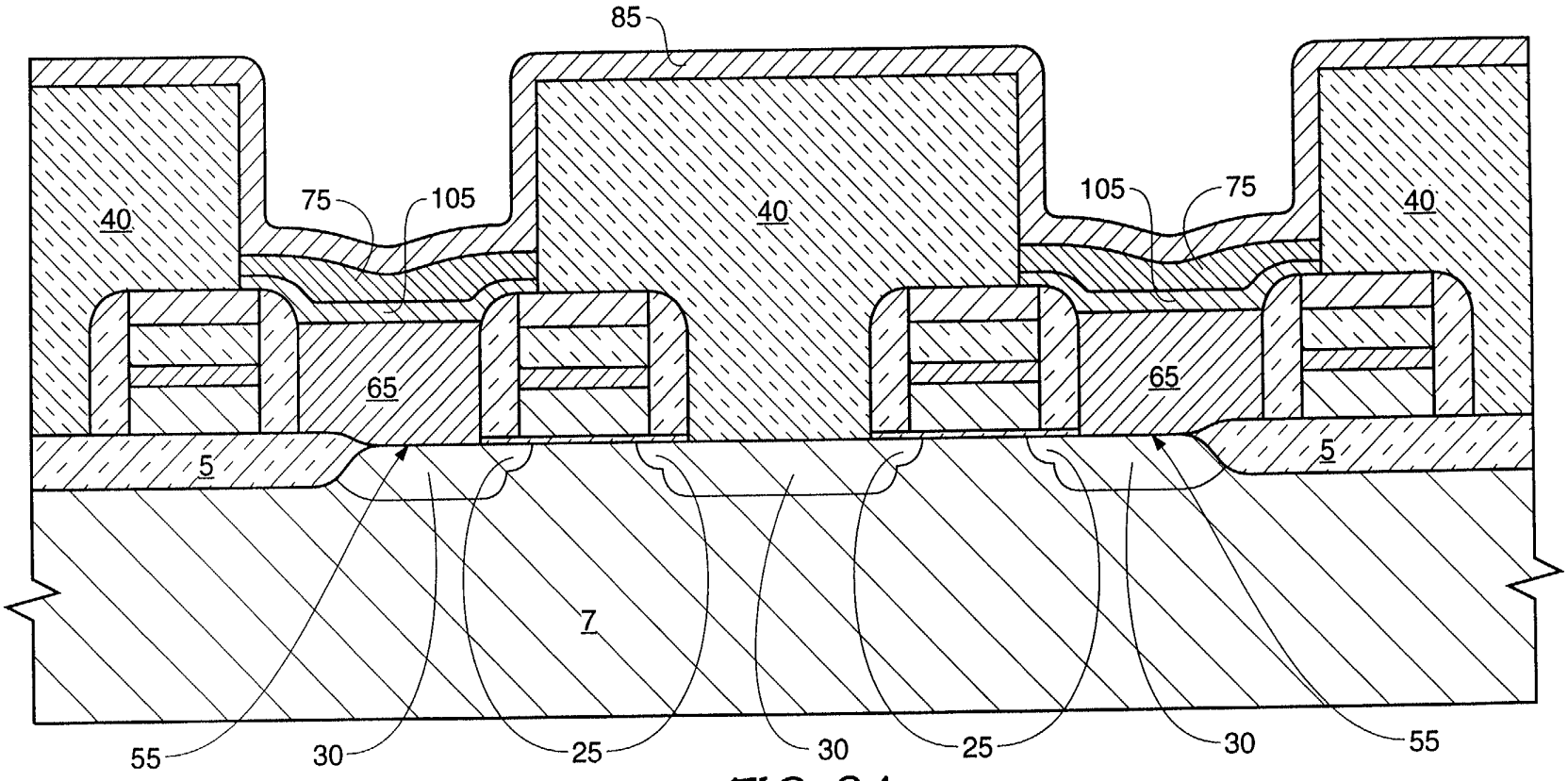

FIG. 24

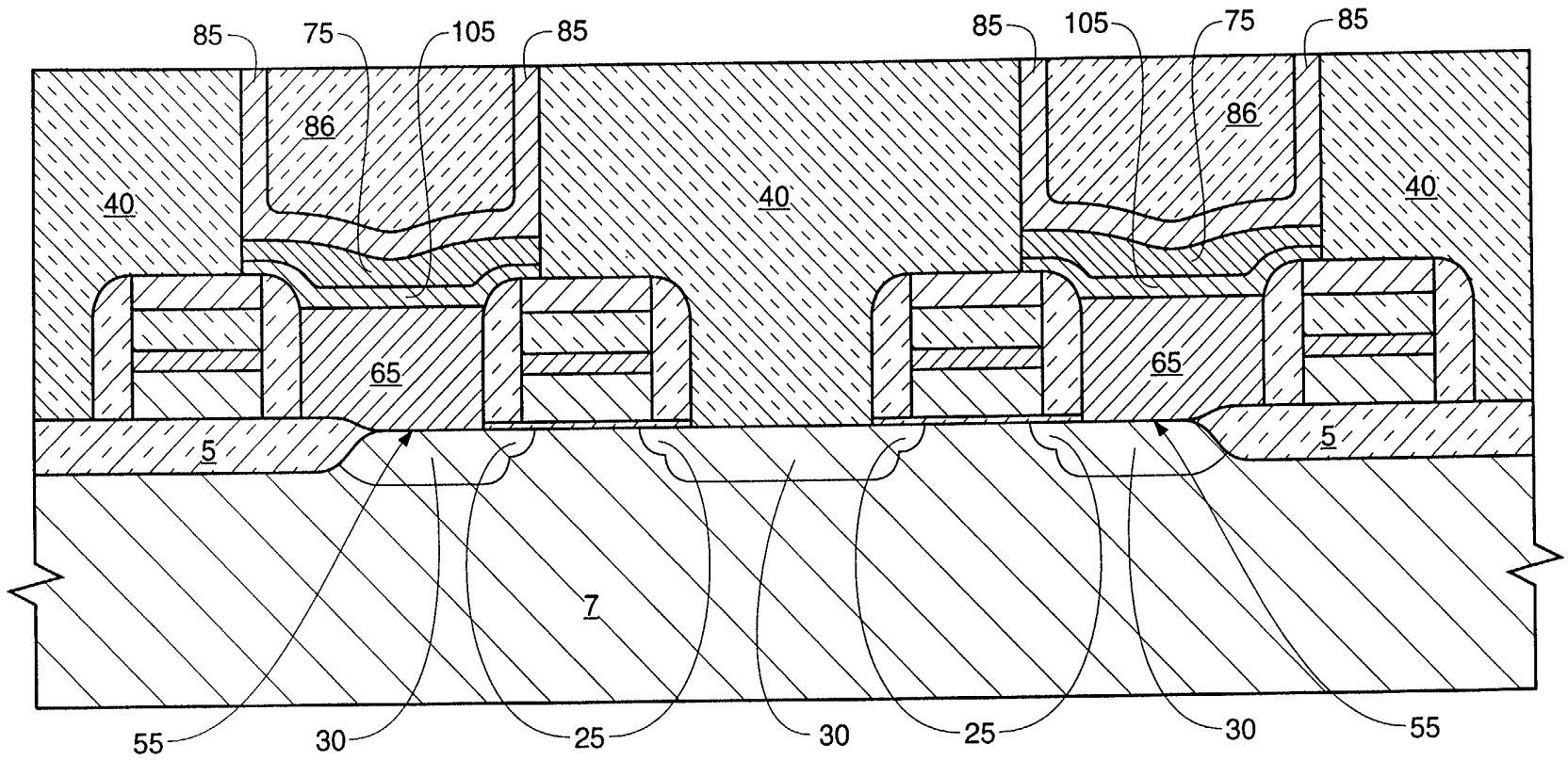

FIG. 25

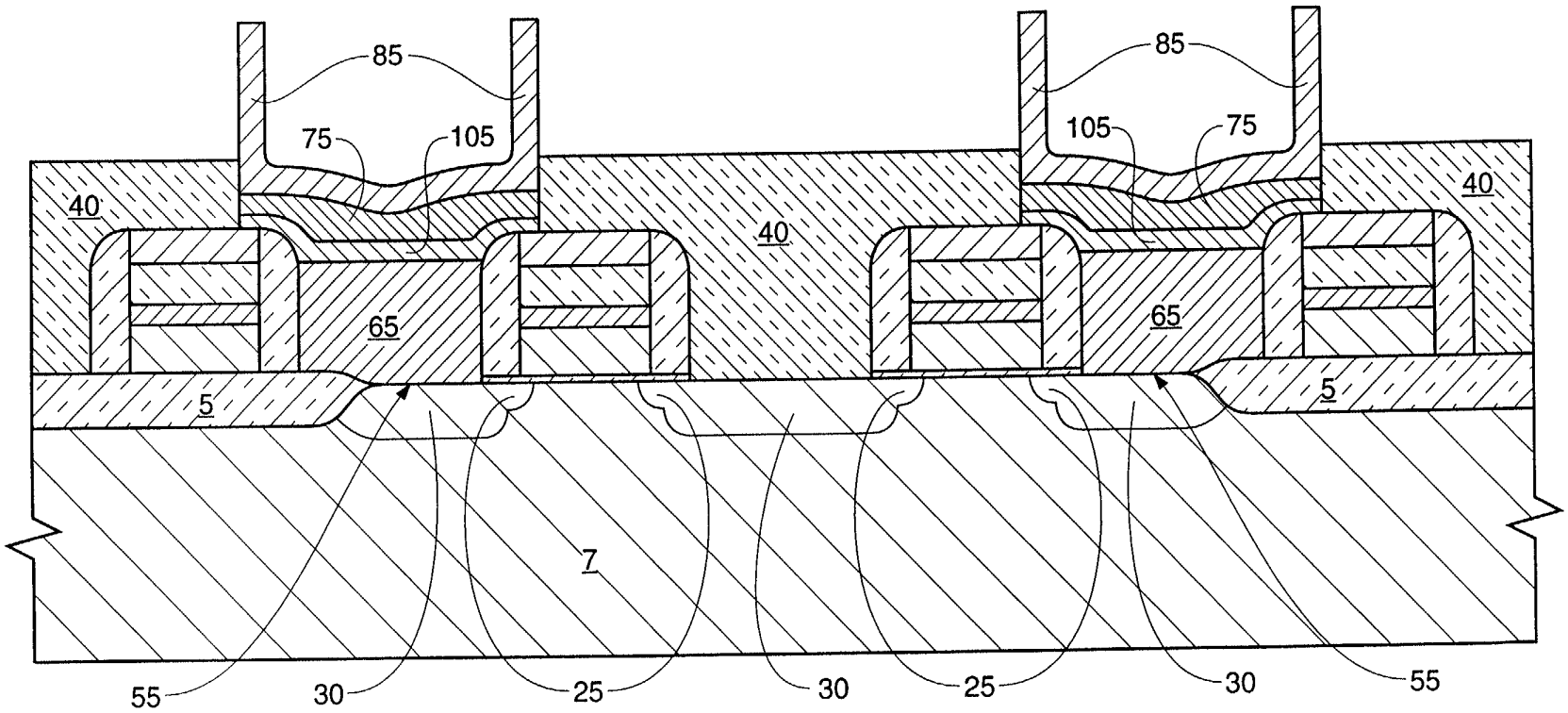

FIG. 26

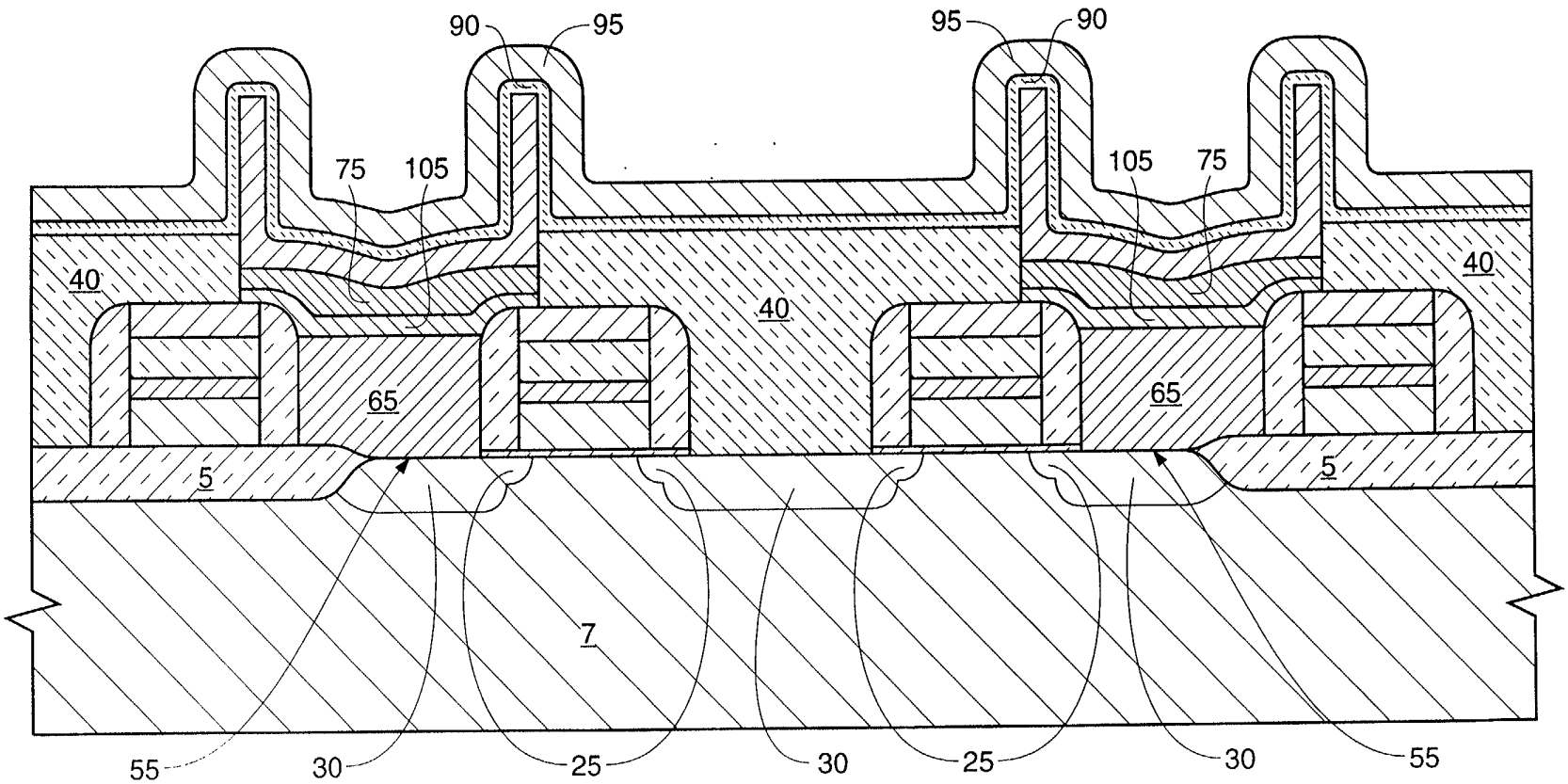

FIG. 27

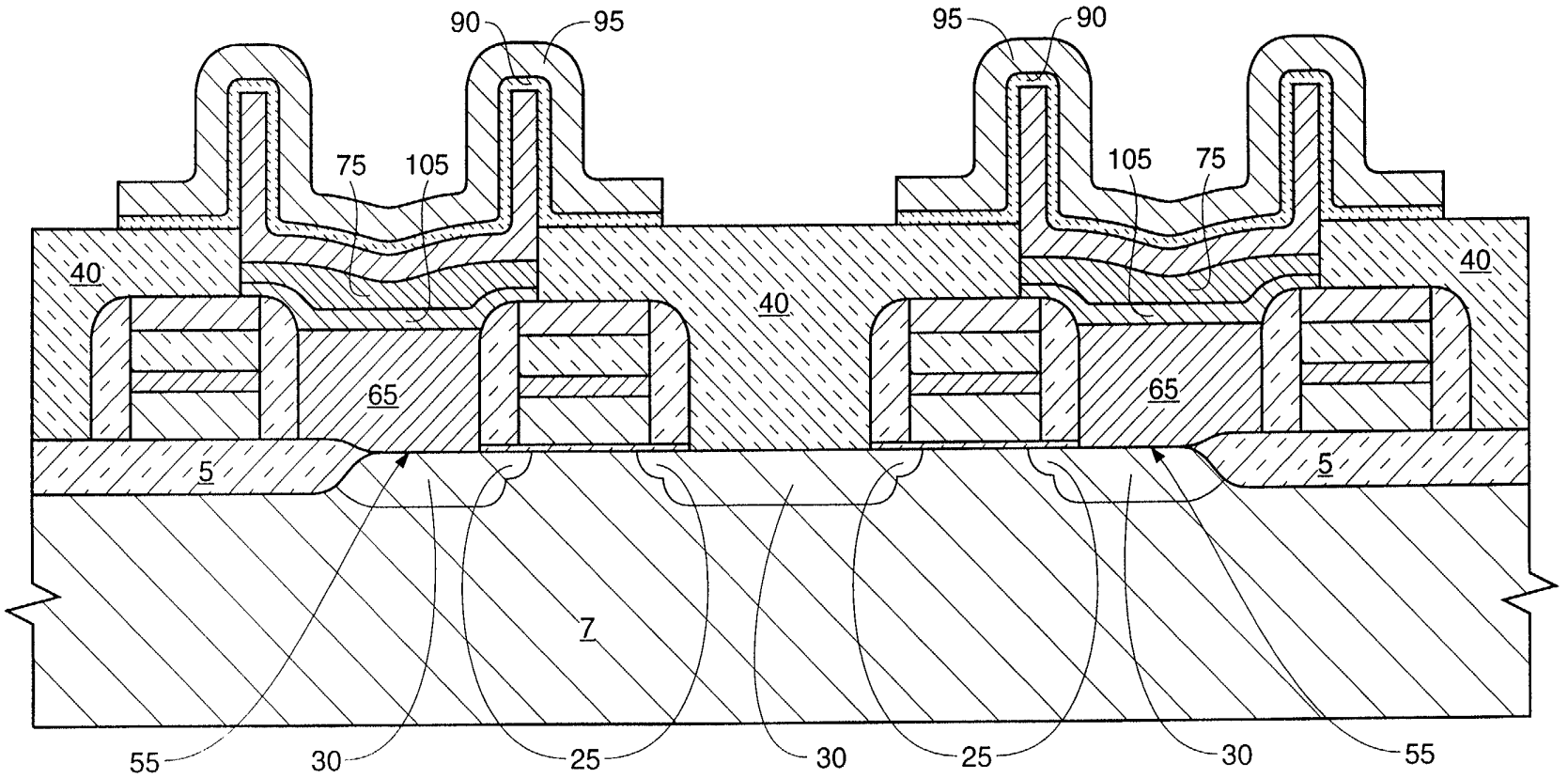

FIG. 28

PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **A METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS**, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I hereby state that I have reviewed and understand the contents of the amendment filed on November 8, 1994 for the above identified specification.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, Section 1.56.

I hereby claim the benefit of any earlier filing date in the United States to which I am entitled under Title 35 of the United States Code, §120 and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 of the United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Susan B. Collier	Registration No. 34,566
Greg A. Blodgett	Registration No. 39,114
Steven P. Arnold	Registration No. 33,354
Lia M. Pappas	Registration No. 34,095
David J. Paul	Registration No. 34,692
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Boise, Idaho 83706

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(208) 368-4514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, Section 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Pierre C. Fazan

Inventor's Signature: _____ Date: 12-14-95
(First, Middle Initial, Last)

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Boise, Idaho 83705

Full name of sole or first inventor: Viju K. Mathews

Inventor's Signature: _____ Date: 12-14-95
(First, Middle Initial, Last)

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City, State, Country: Boise, Idaho, United States of America

Citizenship: United States of America

Post Office Address: 2659 E. Hancock Court

Boise, ID 83706

S/N 08/572,392 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pierre C. Fazan et al.	Examiner:H. Tsai
Serial No.:	08/572,392	Group Art Unit: 1107
Filed:	December 14, 1995	Docket: 303.434US1
Title:	METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS	

REVOCATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In accordance with 37 C.F.R. Section 1.36, M.P.E.P. Section 402.05, 402.07, and 324 please revoke any existing Powers of Attorney, if any, and appoint the following attorneys and/or patent agents to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith:

Bianchi, Timothy E.	Reg. No. 39,610	Holloway, Sheryl S.	Reg. No. 37,850
Billig, Patrick G.	Reg. No. 38,080	Klima-Silberg, Catherine I.	Reg. No. 40,052
Billion, Richard E.	Reg. No. 32,836	Kluth, Daniel J.	Reg. No. 32,146
Brennan, Thomas F.	Reg. No. 35,075	Lemaire, Charles A.	Reg. No. 36,198
Brooks, Edward J., III	Reg. No. 40,925	Lundberg, Steven W.	Reg. No. 30,568
Clark, Barbara J.	Reg. No. 38,107	Lynch, Michael L.	Reg. No. 30,871
Drake, Eduardo E.	Reg. No. 40,594	Madrid, Andres N.	Reg. No. 40,710
Dryja, Michael A.	Reg. No. 39,662	Pappas, Lia M.	Reg. No. 34,095
Embretson, Janet E.	Reg. No. 39,665	Schwegman, Micheal L.	Reg. No. 25,816
Farney, W. Bryan	Reg. No. 32,651	Simboli, Paul B.	Reg. No. 38,616
Fogg, David N.	Reg. No. 35,138	Slifer, Russell D.	Reg. No. 39,838
Forrest, Bradley A.	Reg. No. 30,837	Viksnins, Ann S.	Reg. No. 37,748
Harris, Robert J.	Reg. No. 37,346	Woessner, Warren D.	Reg. No. 30,440
Hofmann, Rudolph P., Jr.	Reg. No. 38,187		

Serial Number: 08/572,392
Filing Date: December 14, 1995
Title: METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS

CERTIFICATE UNDER 37 CFR §3.73(b)

Micron Technology, Inc. hereby certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of an assignment from the inventor filed May 31, 1996 and recorded on Reel 7970, Frames 0325 - 0328. To the best of my knowledge and belief, title is in the assignee, Micron Technology, Inc..

Pursuant to 37 C.F.R. §3.73(b) I hereby declare that I, Michael L. Lynch, am empowered to sign this certificate on behalf of the assignee, Micron Technology, Inc..

I hereby declare that all statement made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true.

Please direct all correspondence in this case to:

Schwegman, Lundberg, Woessner & Kluth, P.A.
P.O. Box 2938
Minneapolis, MN 55402
Telephone No. (612)373-6900

Date Aug 27, 1997 By _____
Michael L. Lynch
Title:Chief Patent Counsel